A Study On Resistive Switching of MgO ReRAM Devices

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Abstract

The inquiry of this dissertation was the development of a memristor device for ReRAM applications. All two terminal devices which show resistive switching and are non-volatile memories are memristor devices. ReRAM devices pose a challenge for successful CMOS integration due to their high variability of switching parameters, which to date is not fully understood. This experimental design is focused on providing insights into this reoccurring problem of ReRAM devices. A ReRAM device was fabricated using MgO in the form of a metal-insulator-metal structure as Pt/MgO/Ta/Ru; by magnetron sputtering and the use of a shadow mask. The fabrication process resulted in four samples with different thickness of the MgO thin film. The samples were study in a two-step process. The first step involved a series of I/V tests undertaken to investigate, resistance ratios, switching cycles, and statistical distribution. The second step applied a percolation model based on circuit breakers to simulate the internal behaviour of a dielectric. Both steps allowed for an in-depth study of the MgO ReRAM devices. The results reveal that an optimum thickness of 30nm is the most consistent in providing reproducibly of approximately 1000 switching cycles, high resistance ratios of 1000 and SET/RESET average voltages of 2.9V with standard deviation of 1.2V and 0.9V with standard deviation of 0.4V respectively. Simulated studies indicated that an increased number of defects ranging from 5%-10% would allow for a switching voltage of approximately 2V for an electroforming process. The simulations also reveal that there can be the possibility of more than one conductive filament present in materials at one time and that all filaments had the appearance of a dendrite structure. The filament presence and structure added a complexity to the switching process which eventually led to variations in switching parameters. Both experiments and the RCB model showed the thinner insulators used in devices will have reduced switching parameters. This study was able to identify the causes behind the large variability of switching dynamics seen in ReRAM devices.

I dedicate this study to my parents and my brothers Colin and Neil.

"To all things complex, lies the most simplest of answers" TRP 97'

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Part I
Introduction

Processing power of computational systems is increasing at a pace that becomes more demanding than there is existing technology to suffice it; and the cost of this computation is directly related to energy. This increasing energy usage led to computational methods evolving from the vacuum tubes to transistors and then to integrated circuits. Integrated circuits with n-type metal-oxide semiconductor (NMOS) and complementary metal-oxide semiconductor (CMOS) design. It was realized that circuit design of smaller sizes possess more processing power using thereby, less energy. This idea led to attempt to understand the sub-micron world and to compare it with the brain[10]. In the 1980s there was a proposal for a type of computing called 'neuromorphic computing', although neuro-computing has been around before [11]. Neuromorphic computing uses very large scale integration (VLSI) systems to imitate the biological brain through analog circuits. The brain has the ability to achieve fast processing power of minute energy cost. The processing power of the brain supersedes any known technology ever developed, and it does this by the neuron ability to perform complex computation through synapses. There exist 10^{16}synaptic processes within the brain which consumes a power usage of only a few watts. There is an emerging technology gaining vast attention that has arisen to address the significant challenges faced by von Neumann computers and that of Big Data. It is a form of neuromorphic hardware called 'memristors´ [2].

Memristive devices address scalability and power usage and have the ability to compete with the processing power of the brain. They can be bio-inspired neuromorphic circuits, that when considered at a nanoscale they have the number density to match the synaptic activity achieved by the brain [12]. Memristors also exhibit nonvolatile memory.
Acknowledging the needs for existing technology such as high speeds and high density memories to address Big Data, there have been a plethora of studies done on nonvolatile memory. The most used memory device is the flash memory, followed by static random access memory (SRAM), and dynamic random access memory (DRAM) all of which are CMOS based. Flash memory being the most popular can be divided into NAND and NOR categories. Current Flash memory suffers from leakage currents that affects its endurance and causes degradation. They are also approaching their scaling limit. Thus, the motivation came to develop a nonvolatile memory with emphasis on high-density and high speed operation [13]. Nonvolatile memory devices research began in the 1960s and there were many postulates but there was no practical application. This came in 2002 by Zhang et al, who showed that a resistive random access memory (ReRAM) device can be successfully incorporated into a CMOS system. There have also been other successful candidates to show practical application. These are phase change memory (PCM), magnetic random access memory (MRAM), ferroelectric RAM (FeRAM), among others. Despite the many explorations in nonvolatile memory devices there is one candidate that successfully outperforms the others, it is the ReRAM devices [14].

ReRAM devices main feature is the ability to be incorporated into CMOS circuits, but it also has other attractive properties that make it one of the best emerging technologies in nonvolatile memory. ReRAM devices are known to exhibit high switching speeds, high density and scalability; they can also be flexible and transparent [14]. ReRAM devices are based on binary metal oxides, and can be fabricated from a quantity

of materials. They are typically made into metal insulator metal structures that are ideal to fit into CMOS technology.

ReRAM devices are still limited in some ways such as endurance when compared to DRAM devices, memory cell area and reliability [13]. Being such a positive candidate address the shortcoming of this type of technology can help address computational limits of today.

1 Types of learning

The ability to learn and how one attains knowledge has pondered on the thoughts of many. The study of biological systems and how they adapt has been widely studied. The reasons for studying how machines can possibly learn is an approach to assist in a complementary way of a broader understanding of the biological systems. The way in which human beings learn and understand can be adapted to the understanding of how we can improve such mechanisms. Notable primary works on the learning process began with Eric Kandel. Kandel described the simplest form of learning as habituation by his observation of the Aplysia's synapse's [9] and with Donald Hebb for synaptic ability.
To obtain a practical manifestation of advanced circuitry for greater processing power, data storage and artificial intelligence one has to employ neuromorphic computing. This form of computing attempts to mimic the neuro-biological process of the nervous system. In neuro-biological systems neural networks are responsible for learning and memory. An adaptation to this computing is called artificial neural networks[15]. The initial step to utilizing learning and memory abilities of the brain begins with synaptic activity. The design of circuits that is based upon neural network systems and their functionality is referred to as a neuromorphic systems [10].

1.0.1 Hebbian Learning

The first attempt to describe synaptic weight was postulated in 1949 by Donald O. Hebb. Hebb attempted to describe the physiological learning rule for synaptic function, later known as the Hebb synapse. It describes the phenomena of the relation between two neuron cells in the brain attempting to learn by exchanging information. Hebb stated " when an axon of cell A is near enough to excite a cell B and repeatedly or persistently takes part in firing it; some growth process or metabolic change takes place in one or both cells such that A's efficiency, as one of the cells firing B, is increased." This form of learning is referred to as associative learning. If two neurons are in proximity, then they are connected by a synapse in-between them. The neurons assimilate communication by a spiking, which in the brain is a membrane voltage. The membrane voltage arises from the differences in polarity between the outside and inside of a cellular membrane. The pre-neuron experiences a spike which is sent through one of its axon's to the synapse interface in the form of neurotransmitters to be received by the post-neuron[9]. Each synapse has a characteristic synaptic weight ω. The synaptic weight has the ability to influence the pre-synaptic neuron spike cumulative action in the post-synaptic neuron. The synaptic weight is susceptible to changes with time, it also displays non-volatile behavior and analog characteristics. Later this theory was revised to spike-timing-dependent-plasticity. This theory of synaptic plasticity encapsulates that synaptic weight can be modulated [2]. Hebbian learning can be shown using spike-timing-dependent-plasticity as a modification rule [16]. In 1996 Gerstner saw the physical use of the Hebbian synaptic modication which is a causality event [9].

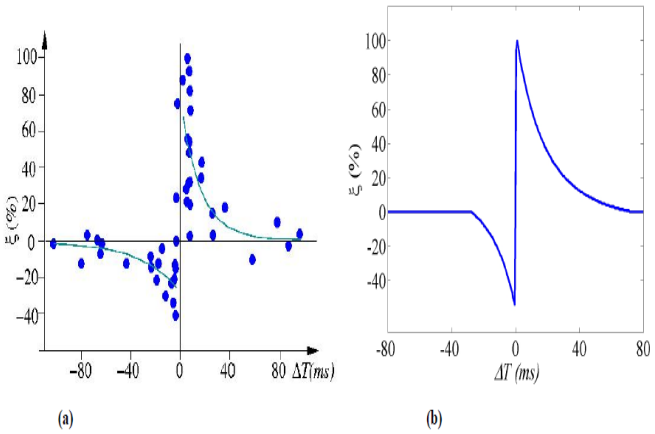


Figure 1: Depicting the correlation between a biological system to an artificial one of memristive behavior. [1]

1.0.2 Spike-timing-dependent-plasticity (STDP)

The single most important biological system that allows for learning and adaptation is the neuron. Neurons are solely responsible for the brains computational abilities through a system called 'neural networks'. Neurons, communicate with each other though a process called synapses. Neurons located in the brain bare a variety shapes, which all comprise of an axon and dendrites structures. More specifically, an axon receives communication and the dendrites serves as a conduit to transfer information to another neuron, this process can be referred to as synaptic activity[16, 17]. A pre-neuron sends a neural spike of voltage towards a post-neuron. The voltage of the neural spike is caused by a difference of the outer to inner membrane voltages $V_{mem-pre} = (V^+ - V^-)_{pre}$. This relation allows for a plethora of membrane channels which cumulative with time. As pre-neuron activity increases it will eventually impose a post-synaptic reaction. This synaptic activity can be described in weighting $'w'$ which provides transmission efficacy formally referred to as the plasticity. The process of synaptic weight is best described by the Hebbian learning. Synaptic weight is non-volatile and analog in nature. The development of describing synaptic weight from Hebb's postulate led to spike-time-dependent-plasticity (STDP). STDP is a temporal relation that is specified to the timing between pre-post neuron spikes, This is characterized as $\triangle w = \zeta \triangle t$, where $\triangle t = t_{pos} - t_{pre}$ and ζ relates to the shape of STDP function experimentally. STDP itself is a form of learning and can be directly related to memristance by the shape of the neural spikes [1, 18, 15]. Neural spikes are colloquially referred to as action potentials. A graphical depiction of neural spikes are compared to generic action potentials for resemblances and prediction are shown in the figure 1 below. The STDP is a synaptic modification which agrees with the Hebbian rule by pre and post synaptic action potentials timing as key to the modifications [9].

2 Memristors and Memristive Systems

In 1971 Leon Chua postulated from a deductive argument that the basic circuit elements were incomplete [19, 2]. Thus came the theory of memristors. Circuit theory states that the three basic circuit elements are the capacitor, the inductor and resistor. The fourth element proposed is the memristor, adjunct to mean memory-resistor [9, 2]became the complement of the existing basic elements. The now four basic elements are related by six distinct pairs of variables comprising of charge q, voltage v, current i, and magnetic flux φ.The relation between them are described axiomatically as:

$$\{(q,v),(i,v),(i,\varphi),(v,\varphi),(i,q),(q,\varphi)\} \quad (1.1)$$

The first five of these relationships were well established in circuit theory.The capacitor relates charge and voltage, the resistor relates voltage and current and the inductor relates current to flux. For natural consistency it was derived by Leon Chua a mathematical relation of charge q to flux φ. The memristor shows behavior patterns involving a nonlinear resistor with memory. On the other hand, the non-linearity property of a circuit element is important for it to be incorporated in an integrated circuit. Non-linear circuits allows for changes in electrical parameters of current, frequency, resistance and so forth as opposed to linear circuits. In linear circuits the output response has a direct relation to the input signal. The memristor is identified as a non-liner element by its electrical characteristics as shown in figure 2.
The properties for the memristor identification remained undetected until 2008, when researchers at Hewlett Packard (HP) labs showed that memristor properties could be observed at the nanoscale for TiO_2 [19]. Memristor properties were enhanced in nanoscale systems showing solid state electronic and ionic properties.

2.1 Theory

The memristor is characterized as a two-terminal nonvolatile device[20, 2]. The memristor relation of charge q versus flux φ shows characteristics that the memristor has a distinct signal processing behavior. A memristor device has a distinguishable identification by the Lissajous loop or commonly known as a '$pinched-hysteresis$'. The pinched hysteresis corresponds to a periodic input signal $i(t) = Asin\omega t$. By a graphical illustration it can be shown for a current i versus voltage v curve but the condition $v = 0$ and $i = 0$ at the same time must occur for any possible value of amplitude A .
The relation of charge q to i and flux φ to v is:

$$q(t) \triangleq \int_{-\infty}^{t} i(\tau)\, d\tau \quad (1.2.1)$$

$$\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)\, d\tau \quad (1.2.3)$$

where q and φ are mathematical identities. Equation 1.2.1 relates charge to current and equation 1.2.3 relates flux to voltage. By a constitutive relation $f(\varphi, q) = 0$ the memristor can be either charge controlled or flux controlled. The relation can be expressed as:

$$\varphi = \hat{\varphi}(q) \quad (1.2.4)$$

$$q = \hat{q}(\varphi) \quad (1.2.5)$$

The terms $\hat{\varphi}(q)$and $\hat{q}(\varphi)$are continuous and piecewise differentiable [21]. By differentiating equations (1.2.4) and (1.2.5) with respect to time the expression for memristance $R(q)$ is obtained.

$$v = \frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq} = \frac{dq}{dt} = R(q)\, i \quad (1.2.6)$$

$$R(q) \triangleq \frac{d\hat{\varphi}(q)}{dq} \quad (1.2.7)$$

The memristance is important as it is the experimental physical property observed when considering the relation of flux to charge. The memristance $R(q)$ at $t = t_0$depends on the past history of $i(t)$ from $t = -\infty$to $t = t_0$. The charge controlled memristor is equivalent to the Ohmic law by:

$$v = R(q)i \quad (1.2.8)$$

The memristor has been termed in a more general sense incorporating state variables ω. This generalized formula considers nonlinear dynamic systems which are used to describe a memristive device.

$$v = R(\omega, i)i \quad (1.2.9)$$

$$\frac{d\omega}{dt} = f(w, i) \quad (1.2.10)$$

The memductance $G(\varphi)$ is also a differential product of equations (1.2.4) and (1.2.5) giving the expression:

$$G(\varphi) = \frac{d\hat{q}(\varphi)}{d\varphi} \quad (1.2.11)$$

The voltage-controlled memristor is given as:

$$i = G(q)\, v \quad (1.2.913)$$

The magnetic flux considered is not a necessary factor for memristance to occur[2]. Hence looking for the memristance by current-controlled aspect is suffice.The latter can be shown graphical as evidential proof of the memristor property occurrence.

2.1.1 Hysteresis fingerprint

For the current controlled memristor the memristance $R(q)$is the slope of the $\varphi = \hat{\varphi}q$ graph. A graph of current i versus voltage v results in a hysteresis being in relation to the memristor identification. This shape is a result of the maxima and minima of the sinusoidal input voltage and current having different values at a point in time [21]. The pinched hysteresis shape occurs because the current and the memristor voltage become zero at the same time.

For positive values of memristance $R(q)$ the hysteresis is always pinched. The hysteresis response arises for any periodic input signal.

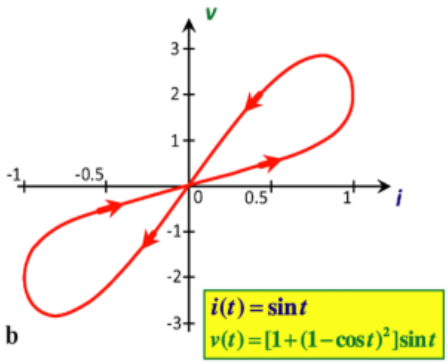


Figure 2: A representation of the ideal behaviour of a memristor as the hysteresis loop. The current-voltage relation are both zero at the origin and the characteristic curve is dependent upon frequency [2].

2.2 Operation of Memristors

2.2.1 Resistive Switching

Resistive switching was observed in 1962 by Hick Mott with binary oxides. It is a process of toggling between a high resistive state (HRS) to a low resistive state (LRS) or vice versa in a dielectric, under the action of a strong electric field. When an electrical stress is applied, the resistive state moves from a HRS state to a LRS and this is referred to as the SET process. Following from the slope of the resistance curve there is an action from moving to a LRS back to the HRS and this process is called the RESET. The resistive switching process is non-volatile and reversible. This phenomena, a type of electrical switching is also seen predominantly in memristive devices[22, 2, 23].

For non-volatile binary memory application there are two memory states, a '1' and '0'. This represents an ON and OFF state for the binary numbers of '1' and '0' respectively. The ON state occurs in the LRS by the process of performing a SET. In the SET process the current is limited. Switching the device OFF requires it to be in a HRS which occurs by the action of a RESET process. The SET process using a threshold voltage that is higher than that of the RESET process. Switching effects are not distinctive from one state to the other but continuous and there can exist intermediate states between the ON and OFF states [19][2].

Resistive switching has two schemes, known as unipolar and bipolar[24, 25, 26]. In unipolar devices, switching does not depend on a change of polarity but rather application of electric fields with the same polarity or increased amplitude of voltage [27]. In contrast to bipolar switching, it depends on opposite polarities to obtain a high resistive state and low resistive state [24].

These variances of switching are present in devices that are based upon their material composition, volume and geometry and the design of the device [9, 2, 28, 23]. They are normally in the form of capacitors with a transition metal oxide in between an active and inert electrode. This description surmises that of a metal-insulator-metal structure (MIM). The phenomena of resistive switching have been demonstrated in simple devices that can be describe as nanostructured, and two-terminal while possessing fast switching speeds [2]. These characteristics are also synonymous with memristive devices and neuromorphic memories. Resistive switching covers

a broad range of nine different mechanism from ferroelectricity tunneling to magnetoresistive memory effects as shown in figure 4. For the metal-insulator-metal structures there are but three redox mechanisms which permit resistive switching. These are electrochemical metalization mechanism, the valance change effects and thermochemical mechanism [25]. With special attention to analog memristive devices for neuromorphic systems the explanatory methods that are relative are valance change, electrochemical metalization and phase change [2].

The development of resistive switching focused on its working principles. This led to resistive switching being studied widely, resulting in many theories, such as conductive filament, Schottky barriers, oxygen vacancy migration, Mott-metal insulator transitions, trapping of charge carriers and interfaces and electrical faucets to name but a few.
A substantial amount of the working principles were focused around transition metal oxides (TMO), a dielectric. The study of resistive switching arose when TMO's were sandwiched between metal electrodes and was observed to exhibit current-voltage hysteresis behaviour. This led to the indication that resistive switching was dependent upon the application of an electrical voltage. Today a vast array of these structures have been reported and are also used to study nonvolatile memory devices[22]. Resistive switching memory devices are known as resistive switching random access memory (ReRAM) devices for their application to memory. They have gained much attention in recent years as these devices are the most considered candidates of emerging non-volatile memory devices, for the replacement of flash memory devices [4, 25, 29, 30, 22]. As previously mentioned current flash memory exhibits high density and low fabrication costs but with growing demands of technology a major factor that would soon be needed is scaling down of these devices. ReRAM devices are promising as they have high-density integration, low power consumption and can be made at low cost. Ideally a replacement to flash memory would require such attributes as possessed by ReRAM devices. There are also other candidates for resistive switching such as ferroelectric and magnetoresistance random access memory as FERAM and MRAM respectively, but these devices pose a problem with scalability [4, 22]. These resistive switching ability have been reported in many binary transition oxides such as TiOx, MgOx, FeOx and NiO and a large variety of materials. It has also been reported resistive switching characteristics seen in perovskite-type complex TMOs and large band gap high-k dielectrics, and in graphene oxides [30].

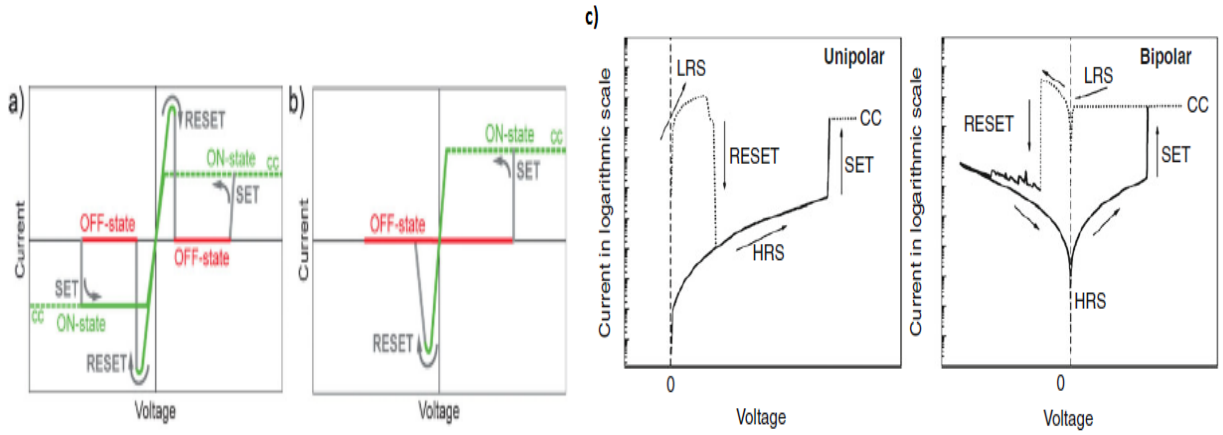
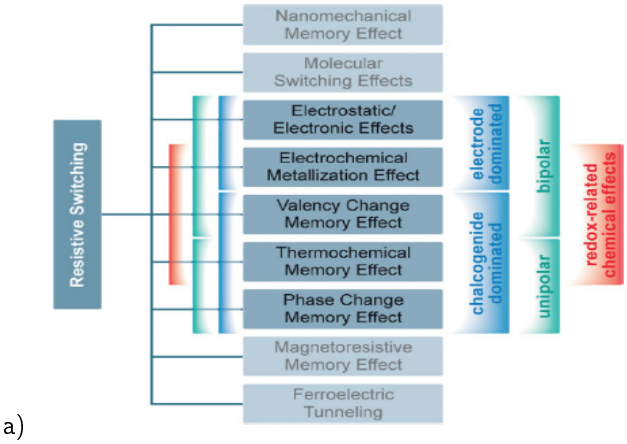


Figure 3: Types of resistive switching, a) shows the process for identifying a SET and RESET. The device state begins in a high resistive state and abruptly changes to a low resistive state, to be ON. The c.c. in b) is the current compliance that is a safety feature to keep the device from reaching a full dielectric breakdown [3]. In c) depicts a clear picture of unipolar states in logarithmic scale that shows with the variance of current the voltage remains in one polarity, whereas in the bipolar depiction shows that voltage has two polarities in accordance of change in current [2].



a)

Figure 4: Classifying memristive devices by a category for resistive switching [4].

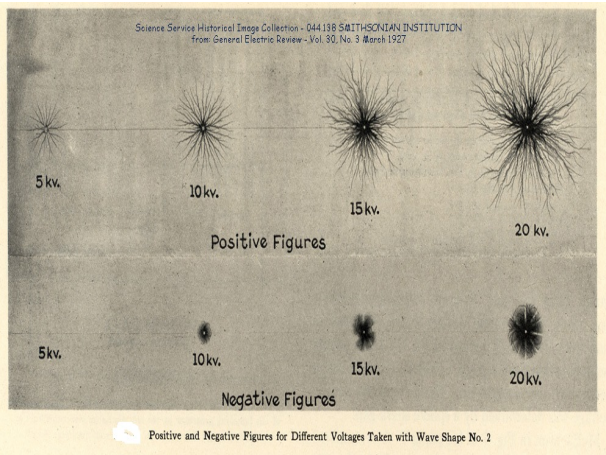


Figure 5: Shows the occurrence of complex stochastic patterns obtained in a dielectric breakdown. This occurrence in solids causes permanent deformation. [5]

2.2.2 Types of resistive switching

Electroforming:

This is the initial step that preconditions the device for switching between SETs and RESETs in succession. It is an irreversible step that occurs with a relatively high voltage bias irrespective of polarity which is applied to the device[28, 24]. This bias is typically larger than the ones that will occur in later stages. When the electroforming step occurs there is a slight breakdown in the dielectric, this is referred to as a soft dielectric breakdown[3, 23]. The breakdown in a dielectrics have been reported to show fractal geometries [31]. The narrow discharge channels that occur in dielectric breakdown resembles the patterns of electric fields seen in lighting storms [5], a depiction is shown in the figure 5. The patterns are stochastic and spread from a wide base to thinner tentacles. These created channels act as passage way for active metal atoms to migrate to the opposite electrode. Dielectric breakdown in solids causes permanent deformation as seen in the figure 6 [23]. This step occurs in such devices as metal oxides, solid stare electrolyte and organic devices[24]. Considering the popularized use of oxides, the electroforming process is essentially a result of electroreduction of oxygen ions and active metal ions [28]. The electroforming process can be eliminated or has a possibility not to occur based on a device fabrication. This elimination can occur in reducing the thickness of the oxide film or by adding an oxygen deficient layer[2, 24]. The electroforming process can still affect a device crucially and offer valuable information.

In each material, there exists different structural deformations during the electroforming process[11, 23]. This makes resistive switching in devices more variable, as many low resistance areas are formed to serve as pathways for electronic conductance. It is proposed that initiating controlled factors prior to the electroforming can provide less variances in different materials. One of the methods are to scale the device to smaller dimensions to increase device density that are comparable to the filament/s formed [11].

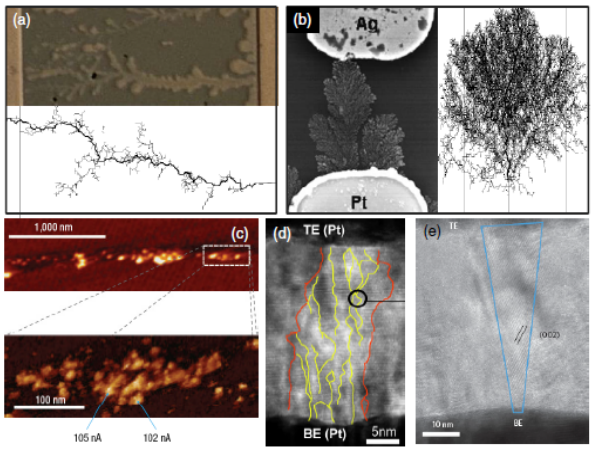


Figure 6: Each picture from a) to e) is an example of filamentary growth in memristor devices In various samples the dendrite like structure is apparent. These deformations are also low resistance pathways that allows for the movement of ions or charge carriers through a dielectric[6].

Filamentary Switching:

To achieve the ON state, from the previous notions there are structural changes which occur within a device. During device fabrication many structural decisions can be manually induced, such as applying defects, defining the geometry of the electrode, and device thickness [32]. However there are structural changes that occur based solely on the material of the device which is synonymous to resistive switching and that is called a conductive filament[3]. This change has been reported to occur as a localized geometrical effect whether in the planar or perpendicular planes of the device cross-section [3, 4]. The conductive filament forming and rupturing is the basis for many resistive switching processes. The existence of the conducting filament has been confirmed both theoretically and experimentally [7, 33]. The presence of the conductive filament has been deemed to cause the variability of many of the switching dynamics associated with resistive switching devices [4]. There are many papers published with the attempt to control the presence of the conductive filament which therein by increases optimization in devices and scalability. Some attempts for controlling the filament growth are seed embodiment, ion irradiation and electrode patterning. Filament growth occurs in two modes, one grows from the active to inert electrode and the other being from the inert to active electrode [23]. The growth of the filament is a self-limiting process affected by an application of a current compliance as shown in figure 3b). A conductive filament is a low resistive percolation path taken as a result, that is caused by the application of a high electrical stress [34]. The conductive filament presence within the device is random and localized as seen by in-situ transmission electron microscopy (TEM) images of figure 6 [6].

The filament structure is taken to be either a solid wire or made of nanoscale minute metals in some cases. It is postulated that there exists only one conductive filament formed, yet multi-filament switching has been reported which occur at the grain boundaries of NiO films [4]. TEM studies involving electrochemical metalization cells (ECM) indicate that there is the presence of several filaments formed but only one central conductive filament predominates. The central conductive filament causes a suppression of other filaments by reduced electric field. Observations made of these additional filaments show that their growth process from one electrode to the other remains incomplete. All filaments have a characteristic dendrite structure

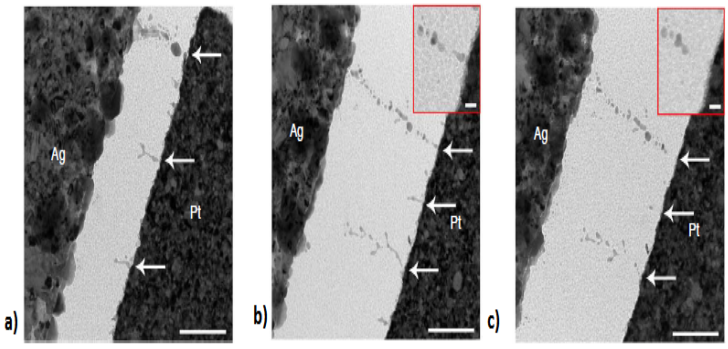


Figure 7: Filamentary growth in material. In a) shows the growth process of a conductive filament towards the active electrode, in b), c) is the dissolution of the filament which cuts the electrical conductive path from one electrode and to the other. The figures a), b) and c) also indicates the formation of multiple filaments [7].

and have been reported to grow from the inert electrode directed towards the active electrode. Alternatively the conductive filament has geometries of a conical-shaped, or bottle-neck shaped structure [7, 6] although upon closer observation also show dendrite like structure. The geometry of a filament is important in the application of consistent resistive switching behaviour as during the write/read operation the creation and rupturing of the filament, which occurs along the thinnest part of its structure [6, 7]. The filament miniature size is due to constraints by the material. As the filament grows it induces a mechanical stress in the material which exerts an equal but opposite on the filament. The filament diameter is affected by Young's modulus, which if higher results in a smaller filament due to the stress factor [35]. Filament growth can be controlled by the application of an electrical stress over time and cation transport process for ECM [35, 7]. For high voltages the filament growth favors a hopping process with a more distinctive dendrite structure and for low voltages filament growth is wider and less restricted. Filaments experiencing high magnitudes of mechanical stress exhibit a wire structure as compared to a dendrite structure [35].
The filaments formed in dielectric devices has shown to influence the write/read process in switching. The thinnest filaments are found near the dielectric/inert as compared to the active electrode. During the write/read or SET process the filament is formed near the dielectric/inert electrode and the erase or OFF process consequently as a dissolution of the filament. This dissolution or rupturing appears in the form of a gap in the filament at the inert electrode. A conductive path is no longer apparent in the device. There remains filaments which are not entirely dissolved that can act as prerequisite for subsequent filament growth. This results in the following write/read process to be of lower threshold voltages [35, 36].

Redox Processes:

Valency change:

Anionic systems involves the migration of oxygen ions across an insulator or more typically, a transition metal oxide between a cathode and an anode. During the forming process at the cathode, there can exist blockages of ion exchanges. This results in an oxygen deficient region that grows towards the anode [23]. This process can be assimilated in the category of valence change reactions [2]. In 2008 HP labs used Ti02 for their memristor device to exhibit resistive switching based upon stoichiometric changes as a result of

oxygen vacancies. Describing the process to the behavior of a semiconductor system oxygen vacancies serve as the donors. The state of the oxygen vacancies within TiO2 causes a modulation on the overall conductance of the device. The most common anionic memristor devices are fabricated from binary transition metal oxides A small class of anionic devices also include high-k dielectrics, large oxide groups, nitrides and chalcogenides [3, 23, 25].

Anionic movement involves the migration of ions that alters the resistance of the material. With a change in resistive state the process of resistive switching has occurred. The prognosis of this is not a singularity effect, related to only material structure but also incorporates a diversity of defects that alter electronic transport. The ability to understand the importance of these two effects would allow for better fabrication and design of a memristor device for optimum resistive switching dynamics [23]. The characteristic switching of anionic devices is bipolar which is not easily discernible. The polarity in bipolar switching is based upon a work function and oxygen affinity, and the polarity of the electroforming process. Initially the resistive switching phenomena was reported to be the effect of electronic transport. The transport mechanism are described in literature as a charge-trap model obeying the Fowler-Nordheim tunneling effects. Where charges are trapped in defects or induced metallic nanoparticles in the dielectric. This changes modifies the electronic barrier and at the interface in semiconductor devices the Schottky barrier [25]. A broader consideration to resistive switching lie by, expanding the concept from electronic transport to transport of anions such as in metal oxides. In metal oxides, oxygen vacancies are more mobile than metallic ions causing substantial change for the electronic state.

Electrochemical Metalization Electrochemical metalization is often referred to as cation-based switching. This form of switching involves forming a conduction path with cations between an active electrode to an inert one. The cations migrate from an electrode that is doped by an electrochemically active material and it moves to an inert electrode. The inert electrode is usually of an electrochemical inert metal such as W, Pt, and Ru among others [37]. The migration of ions occurs via fast ion transport [6]. One example of electrochemical metalization could be explained with the Ag ions. Cations of Ag are transported through a thin electrolyte film by the influence of a high electric field. When the cations reach the inert electrode, crystallization and a reduction process occurs at the electrode/electrolyte interface. In the case of Ag+ ions, dendrites are formed as a conductive filament between the two electrodes [4]. The action of resistive switching occurs with the formation of the conduction path and its dissolution. A conduction path can consist of a conductive filament made here of cations. With the filament making a linkage between the two electrodes the state of the system changes to ON. A subsequent event is the dissolution of the conductive filament which leaves the system in an OFF state.

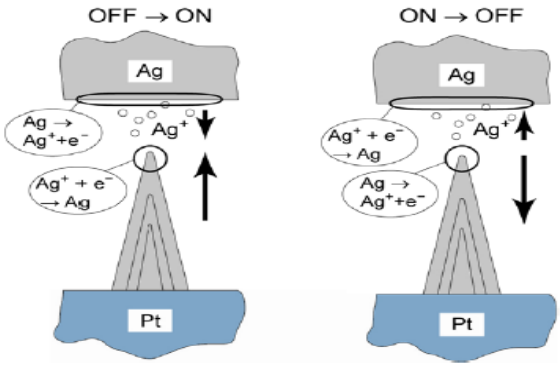


Figure 8: The migration of Ag+ cations from the active electrode at the top. The cations flow towards the inert bottom electrode through an electrolyte and thereby forms a dendrite conductive filament. Once the conductive filament is formed the system becomes ON and as it dissolves the system becomes OFF.

3 Metal-insulator-metal memristors

A memristor device consists typically of three layers, two outer electrodes (metallic) and insulating material in the center. The insulating material used is typically of a transition metal oxide [24]. It is within the insulator that memristor properties occur [11]. Studying the conduction through an insulating material is crucial for the adaptation of memristor devices in integrated circuits. The first approach is to perform sample testing. One type of testing is using a metal-insulator-metal (MIM) in the form of a capacitor or diode. The MIM structure two outer metals are referred to as the electrodes. Connecting probes to electrodes of the MIM allows one to study the electrical characteristics of the device. An asymmetric connection is favored for the MIM capacitors, where one probe is applied to the bottom electrode and the other to the top electrode. Each one of the electrodes, is made from a different material. Having electrodes made from different materials permits for different chemical and physical properties within the MIM device. These varying parameters are such as, work function, that affects the barrier height of metal-dielectric interface and the effective mass, for the amount of charge carriers [38].
The mechanism for the conduction through a MIM is partially due to the electrical properties of the electrode-dielectric interface. This is govern by the electrode/injection limited conduction mechanisms, which have several postulates.

3.1 Magnesium Oxide

Magnesium oxide (MgO) is a compound which is chemically inert. It belongs to the high-gate materials and tt is a binary metal oxide with a high dielectric constant (6-10), band gap (78 eV), thermal conductivity with a breakdown field of (12 MV/cm) [39].
The chemistry MgO, shows that it is a white powdered solid that is odourless, and it has a molecular weight of 40.3 g/mole. Its boiling point and melting point are 3,600 ºC (6512 ºF) and 2,800 ºC (5072 ºF) respectively and its specific gravity is 3.58 at 25 ºC.

The compound MgO consists of a lattice of Mg2+ ions and O2− ions held together by ionic bonding. It crystallizes in a cubic cell with a rock-salt (sodium chloride) structure. The crystal structure can be described as a face-centered cube (fcc) lattice of Mg ions with O ions occupying all the octahedral holes or

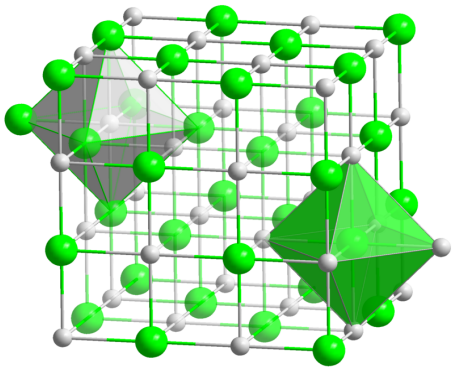
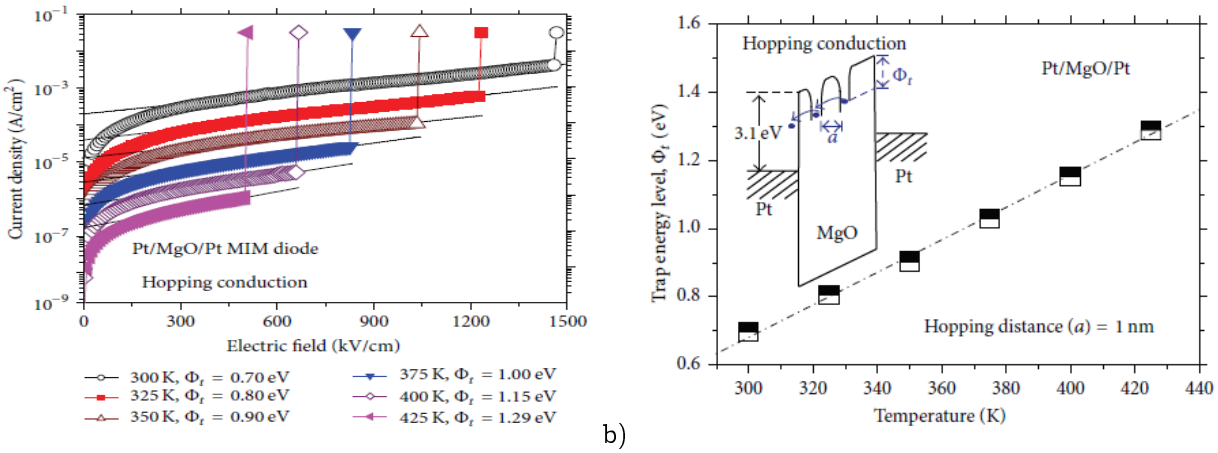


Figure 9: Chemical structure of MgO lattice

vice versa as seen in figure 9. The structure of MgO used is of monocrystalline (001) nature.

Due to the nature of MgO it has a high importance in magnetic tunnel junctions (MTJs), but not only, MgO is highly attractive as a resistive switching layer for ReRAMs devices. The high dielectric breakdown field of MgO thin films may have the potential to ensure adequate band offsets and to reduce leakage currents in device applications in ReRAMs [8]. The conduction mechanism in MgO as a dielectric have been known to be hopping and ohmic conduction in some experiments and to include space charge limit conduction (SCLC) in others [40]. The figure 10 shows the conduction of MgO.
Using MgO films in MIM structures as the insulating dielectric, there is a good migration of ions. Experiments show that there can be either the movement of Mg2+ or O2- ions. It is reported that oxygen ions have a greater mobility when compared to magnesium cations which can favour oxygen ions being the responsible factor for forming the conduction path. When a voltage is applied to the MgO film it was found that oxygen ions migrate towards the anode creating oxygen vacancies. The oxygen vacancies become accumulated in a localized area and this causes a stoichiometric change in the MgO. This change then creates and redistributes low resistances spots throughout the film[41, 42].



a) b)

Figure 10: a) Experimental data and simulation curves of hopping conduction in high resistance state in Pt/MgO/Pt memory device. b)Temperature dependence of the trap energy levels in high resistance state. Inset graph shows the band diagram of hopping conduction in Pt/MgO/Pt memory cells [8]

4 Percolation Model

Resistive switching MIM structured devices are widely known for their vast disparity in switching parameters. The statistical distribution of switching dynamics is wide and hinders the device from achieving practical implementation. The ability to control the ReRAM devices can provide enhanced high reliability and reduce variability. Due to the nature of statistical variation in these devices an analytical model can be used to describe its behaviour and improve understanding [43]. Percolation theory is considered in ReRAM devices due to the nature of the electrical switching in the device by a conductive filament along a percolation path. Particularly ReRAM devices using oxides, there is a well-known percolation theory that describes dielectric breakdown of its random nature. Percolation theory refers to the aggregation of clusters in a 3 dimensional graph. It is a mathematical model that can be applied to non-linear physical systems to make predictions about the behaviour of the system.

Percolation theory has many models. The common most models utilize a lattice formation in a cuboid shape. It assumes that the lattice can be randomized by causal selection of bonds or 'edges' of the lattice with a statistical probability p. This approach to explain the behaviour of systems by a lattice can be classed as a site percolation threshold or bond percolation threshold [44], see figure 11 for an example. Bond percolation assumes systems over a lattice of $L = L^d$ for d dimensional Euclidean space. It can be defined as a lattice with bonds that can open given a probability of p or close given a probability of 1-p that is occupied at random. This is often referred to as the Bernoulli percolation. Bernoulli percolation can be expanded to encompass other systems that are continuous such as the Poisson method.

There are many percolations models used to explain the random nature of resistive switching in memory devices. One of these models is to consider circuit breakers in a lattice formation. This model became popularized to explain resistive switching oxides used in MIM structures. It is called the random circuit breaker network model (RCB), which is a simplified approach of using the percolation theory [45]

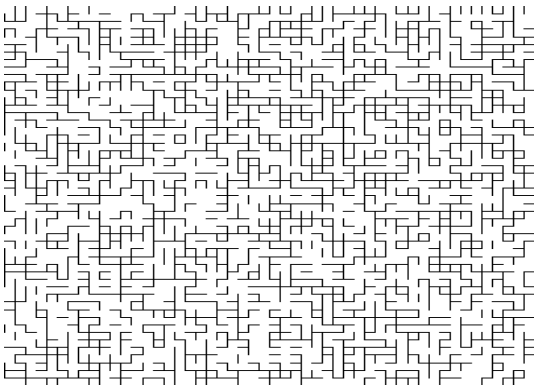


Figure 11: An example of bond percolation for a lattice with probability p = 0.51.(Bond percolation p 51" by de:Benutzer:Erzbischof - Own work. Licensed under CC BY-SA 3.0 via Commons)

5 Conclusion

Flash memories are quickly approaching their scaling limit and there is a plethora of emerging technologies to replace it. ReRAM devices are showing the most promising ability to replace flash memory as the future for non volatile memory[45]. These devices can be a form of memristors. Since the discovery of the memristor by researchers at Hewlett Packard labs in 2008, interests have grown within the scientific community to understand and seek applications for these devices. One reason for the growing interest is the a property of memristor known for its high memory density. When compared to flash memory the memristor can out perform this class of memory devices. Not only is the memristor a good candidate for memory applications, it can be applied to the understanding of biological learning mechanisms and its scaling size is much smaller as compared to other devices.

The functionality of the memristor allows for vastly improved devices on micro-chips in integrated circuit, increasing its parallelism and enhances the value of learning versus programming. In the latter the ability for automated systems to make predictions and off decision making becomes a possibility [46].

Memristive ReRAM devices can have many benefits but some are hindered by the resistive switching mechanisms, which is not yet understood. Thus a study to undertake the resistive switching dynamics is important for future practical applications.

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Part II
Experimental Techniques

6 Deposition and Fabrication of MgO thin films

The fabrication of metal-insulator-metal devices for resistive random access memory applications were devised in Lisbon at INESC-MN. The techniques used were, deposition and microfabrication. A total of four samples of different scaling measures were fabricated for study.

6.0.1 Magnetron sputtering

INESC.MN PVD-Magnetron which is fully automated, Nordiko 200 was used in the deposition of MgO thin films on SiO/Si/SiO/Ti (25nm) substrates.

In general description, deposition is a chemical or physical process that comprises of a wide range of techniques for the fabrication of thin films. Sputtered films using a magnetron, is one of the most recent deposition techniques that has superior performance when compared to other deposition methods. It is a form of physical vapor deposition (PVD). Magnetron sputtering can be applied in low-friction coatings, corrosion-resistant coatings, and coatings exhibiting optical and electrical properties as thin films.

The sputtering takes place inside a vacuum chamber. This vacuum chamber is filled with an inert gas such as argon Ar or xeon Xe. Inside the chamber a target is connected to a negative bias, sometimes referred to as a cathode, that becomes bombarded by a plasma. The plasma contains energetic ions which strike the target, causing the target surface atoms and secondary electrons to be removed. This is referred to as sputtering.
The magnetron operates under the influence of a magnetic field as shown in figure 12. The field is placed in relation to the target so prevent secondary electrons migrating towards a substrate. The electrons will follow the path of the magnetic field lines in a spiral position. When the electron mobility becomes restrained by the field this increases the ionized electron - atom bombardment which results in increased ionisation efficiency. The increase of this efficiency produces a denser plasma that increases the ion bombardment on a target, giving faster sputtering rates, and better deposition times. In general the operating pressures for this conditions are 10^{-3}mbar - 10^{-2}mbar and -500V[47].
The deposition process of our MgO sample started with the oxide being from a monocrystalline (001) structure. The deposition was performed for varied levels of thickness ranging from 15nm, 22.5nm, 30nm, and 40nm of the oxide. The sputtering occurred at room temperature with a base pressure of $2x10^{7}$ torr 9 sccm and an Ar flux of 185V.

6.0.2 Microfabrication

MgO thin films were used an the insulator/dielectric in the MIM as a ReRAM device. The structure of MgO used is of monocrystalline (001) nature. It was used in correlation with Platinum (Pt), Tantalum (Ta)

and Ruthium (Ru). Typical of MIM structures there is an active electrode and an inert electrode. Here the active electrode is Ta as the top electrode and Pt as the inert bottom electrode. Ru acts as a guard to prevent oxidation of Ta. MgO was sandwiched between the electrodes to form the structure Pt/MgO/Ta/Ru. The bottom electrode was fabricated using magnetron sputtering, the top electrode was fabricated using lithography.A schematic of the MIM structure using MgO is shown in figure 13 a) and b).

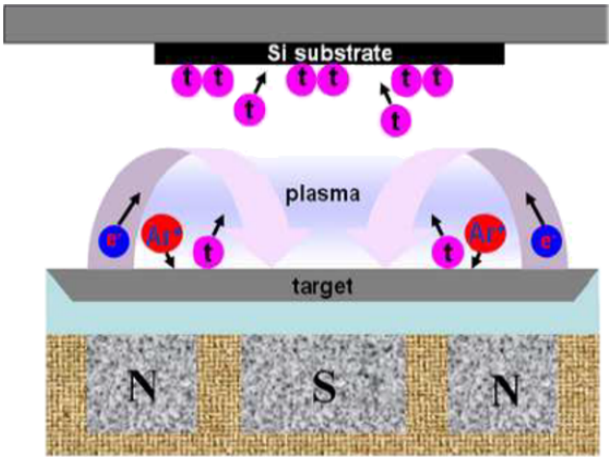


Figure 12: Conventional magnetron, with magnets at the base of the target which influence the plasma concentration.

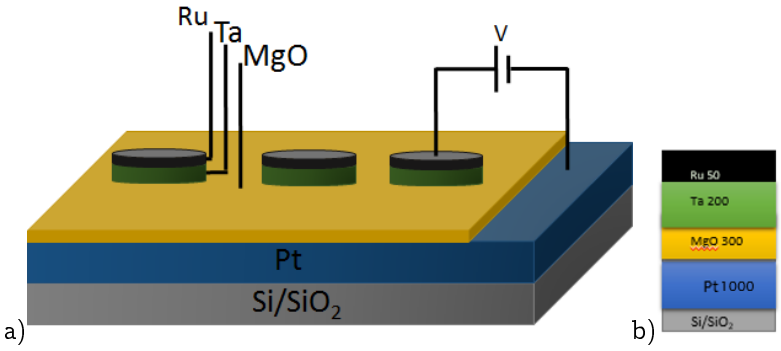
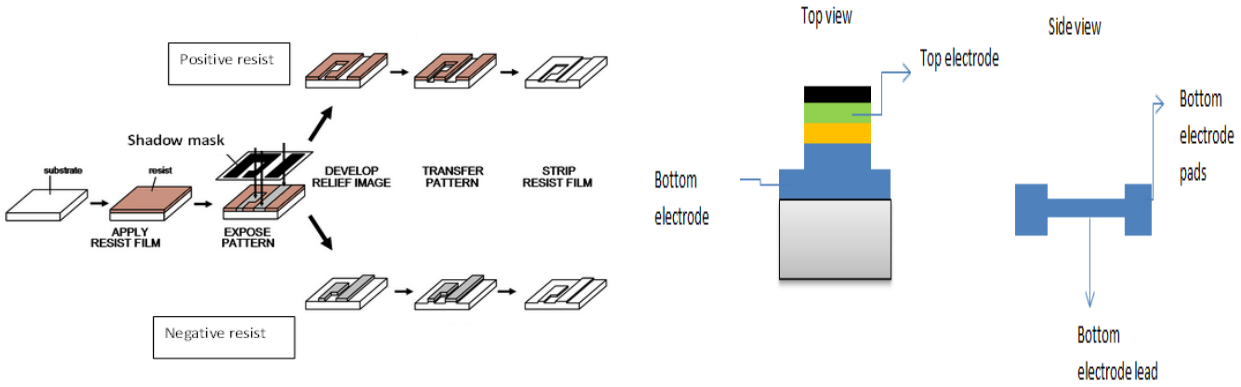


Figure 13: A schematic of MgO ReRAM device in the form of a MIM structure.



a) b)

Figure 14: Shows the schematic of an etching and lift off process

The top electrode lithography was performed using direct write laser (DWL) 2.0 Heidelberg optical lithography machine. The process begins by using vapor prime for a run time of 30mins. The first step is the wafer dehydration with conditions at vacuum, 10 torr, N2 inlet at 760 torr and heating the samples at 130ºC. Then the samples underwent priming in a vacuum at 1 torr, for 3mins and place in hexamethyldislazane (HDMS) at 6 torr for 5mins. A purge prime followed by placing the samples in vacuum at 4 torr for 1min then 2min. Finally each sample was returned to atmosphere conditions by N2 inlet at 3mins.
The second step in the lithography process involved coating the samples with a photoresist of $1.5\mu m$. The first step of the coating began with dispensing the photoresist on the samples by spinning at 800rpm for 5 secs. This was followed by a second spin at 2500rpm for 30 secs. for a thickness of approximately $1.45\mu m$. The samples were then soft baked at 85ºC for 1min. The photoresist either protect the patterned areas from the Ion Beam Milling (etching) process or give way for new patterned layers This is depicted in the figure 14.

The etching process was done using a Nordiko 3600 for the top contact. The etching of the sample was done at 60 degrees and cooled for 200 secs as shown in the figure 14 b). In similar fashion this could have been repeated using a lift off method. The etching gun operated at 160W, for a current of 105mA +750V/-350V at 12sccm Ar. The etching was stopped before the bottom electrode vanished.

After these steps the samples were prepared for patterning. A pattern was designed using a computer aided design (CAD) program and loaded into the lithographic system. Then the samples were arranged to apply a shadow mask. Shadow masks are a pattens of the microscale which expose film areas for deposition. The shadow mask was constructed to have 36 apertures each of $300\mu m$ in diameter. After exposure, the samples were then developed by baking at 110ºC for 60secs and cooled at 30secs. A developer was then added for 60 secs to the samples to remove non exposed photoresist. When this was completed the photoresist thickness was checked using a profilometer.

6.0.3 Transport Measurements

To undertake studies of I/V characterisation the workstations provided by IFIMUP were used to perform tests on the MIM MgO samples.

Direct current (DC) electrical measurements were undertaken in an asymmetric configuration using tungsten micro-probes that were connected to a Keithley sourcemeter 2400. All the measurements were performed at room temperature. A voltage sweep was applied to the top electrode with a grounded bottom electrode. A positive bias was defined for current flowing from the top to the bottom electrode. The voltage sweep was applied as $0 \rightarrow V_{max} \rightarrow 0 \rightarrow V_{min} \rightarrow 0$ with Vmax as the positive bias and Vmin as the negative bias and had voltage steps of δV^+,δV^-. There was a time delay of $\delta t^+, \delta t^-$that coincided with the different voltage biases. This time delay is the duration between each voltage step applied. A depiction of the step voltage is shown in the figure 15.
A current compliance for both polarities was applied to protect the sample from experiencing an overshoot and complete dielectric breakdown.

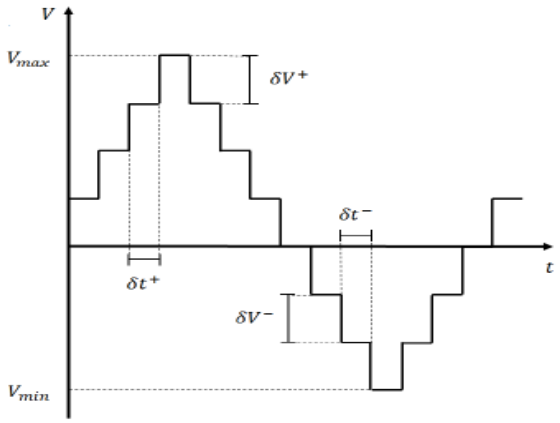


Figure 15: Displaying the voltage step process by time delay

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Part III
Electrical Characterization of MgO Memristor Devices

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7 Classification as a Memristor

Introduction:

Metal-Insulator-Metal (MIM) structures were studied as a proposed memory device. They were fabricated using magnetron sputtering for four test samples of different MgO thin film thicknesses. The samples were named S1 at 15nm, S2 at 30nm, S3 at 22.5nm and S4 at 40nm. Each sample contained a total number of 36 individual memristor devices. Some of these devices were chosen at random and tested under similar current/voltage (I/V) conditions to obtain the signature pinched hysteresis loops, one of the tools used to identify a memristor. Once the device exhibit memristive behaviour, it was further tested to see its endurance. Under this analysis the following were considered, conduction mechanisms, SET/RESET fluctuations, cell performance, delayed time effects and scaling.

7.1 Experimental Results

7.1.1 Classification as a Memristor

Current –voltage characteristics of MgO were obtained to verify if the sample exhibit a pinched hysteresis loop. A signature of memristor devices, the hysteresis loop shows current and voltage both equated to zero at the origin. The figure 16 a) on the left shows the ideal memristor behaviour as compared to the experimental result of MgO memristor device figure 16 b). In the MgO memristor device the input source was a step voltage input v(t) which imposed a response of a current I (t) of the same frequency, the locus (v(t), i(t)) was shown to be zero when v(t)=0. This made the device a voltage-controlled memristor. When a continuous input is applied, providing that all the locus points of voltage and current have identical zero crossings the device is described as a passive memristor. Once the device maintains this behaviour it obeys the fundamental property of a memristor which states that "once it is pinched it is a memristor". An ideal memristor is shown as reference of the pinched hysteresis behaviour.

It is also noticeable that the figure 16 b) is an odd function and follows a counter clockwise direction. This obtained experimental graph shows from step 1 to 2 the device in a high resistive state (HRS), at point 2 there is an abrupt change in current that changes the resistance state of the device at point 3. The device is now changed to a low resistive state (LRS) at point 4 under the imposed current compliance (c.c). The c.c. is manually set by the user to prevent the device from experiencing any damage such as an electrical overshoot from the source meter, or full dielectric breakdown. Proceeding point 4 at points 5 to 6 the device maintains a LRS state until point 7 where after an abrupt current change the device returns to a HRS at point 8. The entire process is that of performing a SET and RESET as shown. The SET process allows for a resistance

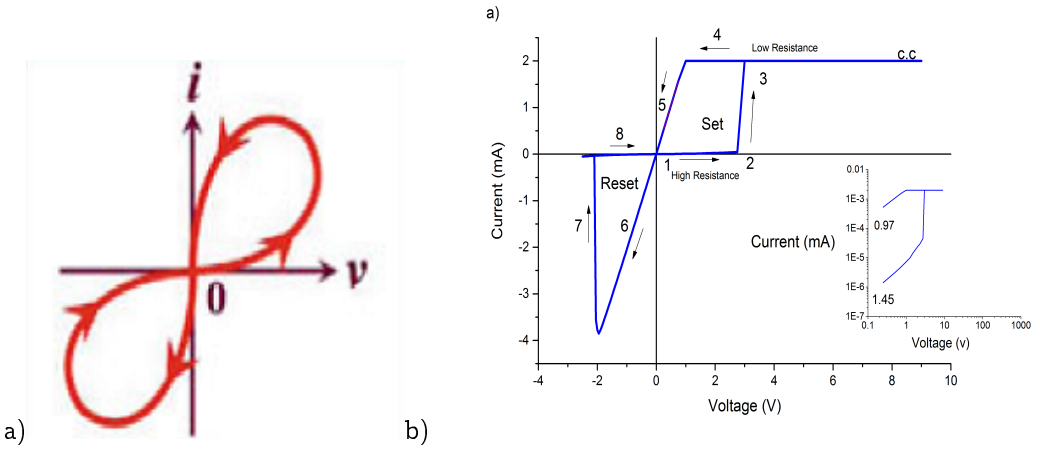


Figure 16: The graph on the left shows the ideal behavior of a voltage controlled memristor, it is odd symmetric and the loci of the voltage and current are both zero at the origin[9]. In figure b) is an experimental realization of memristive behaviour by the signature pinched hysteresis loop. It shows 8 points where at each point indicates a change of state in the material. The inset shows a log-log scale of the same iv curve.

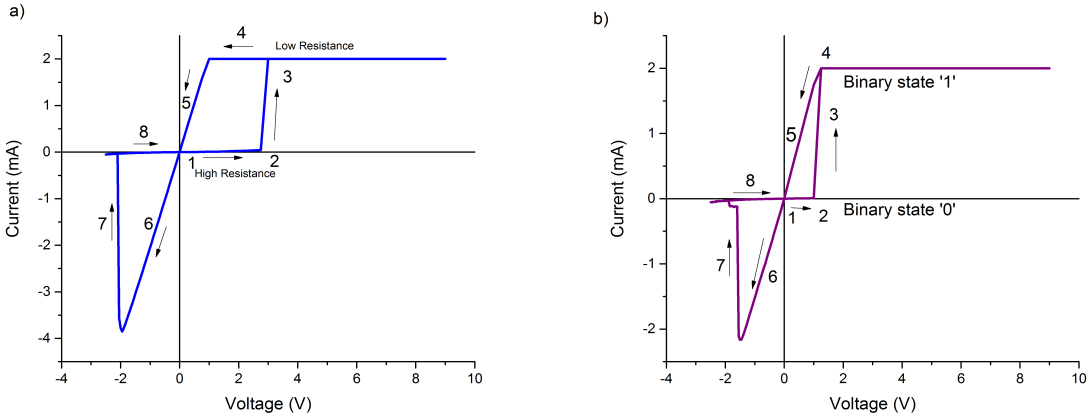


Figure 17: Hysteresis loops obtained for sample F under the same conditions the hysteresis loops can appear differently. On the right also indicates the two states of the MgO memristor device.

change for HRS to LRS by an abrupt increase in current. While the RESET by an abrupt decrease in current reverts the resistance states from LRS to HRS. This can be repeated by applying an external voltage sweep.

Applying a log-log scale shown in the figure..b), to understand the conduction behavior, there is ohmic behaviour with a slope of 0.97 upon a gradual increase of voltage from 0.25V to 1V for the ON state and a space charge limit conduction (SCLC) slope of 1.45 upon a voltage decrease of 2.25V to 0.25V to the OFF state. A physical adaptation of the ideal memristor behaviour indicates that even under the same conditions no two hysteresis curves are exactly the same. This is a result of different initial states, as seen in figure 17 a) and b) [48]. For the same maximum input voltage of 9V and 2mA current compliance the resulting figure17 differs from one another.

The slope of the two figures 17 a) and b), numbered as point 5 differs by their high resistance state to a

low resistance state under the same input frequency. The slope of the hysteresis loop is referred to as the resistance. The conduction of in figure a), moves from 486Ω to 1.6 x10^5 Ω at -0.5V to 0.5 respectively. Similar behaviour is observed for figure 17 b). Once the resistance state changes, it can be used as an electrical switch. If the memristor has a smooth input function used here as the input voltage then a continuous number of resistances and not only binary states can be obtained. A binary state of '0' is apparent in both figures 17 a) and b) from points 1 to 2 and a binary state of '1' appears at point 4 on the figures 17. The admission of the binary states is referred to as the 'write' function. This function occurs by the application of a programming voltage. Memristors that are used as resistive switching devices, should have write voltages be approximated to a few mV, if they are to be comparable to flash and other forms of memory [23]. A write function is used to turn the memory device from an OFF state to an ON state. Specifically here in the MgO memristor device the resistive switching is shown by moving from a high resistive state to a low resistive state. This resistance state is that of the MgO thin film, where ions are known to move rather freely. The film's resistance is reliant upon the direction of the charge which passes through it. This is reversible by changing the direction of the current [49]. This phenomenon is seen in the graphs giving the signature hysteresis shape. Memory states of '1's and '0's are halted as the power in switched off in typical volatile memory devices, on the other hand in memristors they are non-volatile. Non-volatility is a property of retaining a state when an external power source is switched off [20]. According to new fundamental theory on memristors non-volatility is not a necessary factor to classify a memristor [48]. Memristors can be classed as a type-A or type-B memristor that is based on the switching behaviour. Type A represents the ideal memristor of curved pinched hysteresis loops, whereas in type B memristors have a triangular pinched hysteresis loop. Type B memristors also have a high ohmic conduction with a straight line I-V graph [9] seen here in figure 16 b). Observing the MgO sample it can be classed as a type B memristor. As the fundamental theory of memristors has been expanded to include classes of extended and generic memristor, the above tested MIM structure using MgO can be classed as a generic memristor as all the hysteresis loops are not odd symmetric and tend to a straight line given the applied input step voltage. There was a repetition of the SET process after an applied step voltage pulse and in this manner, memory can be achieved by switching between a LRS to HRS.

7.1.2 Resistive switching Characteristics of MIM

Electrical Characterization: The study for I/V characteristics begun by the use of a voltage scheme defined in a LABVIEW program. This was performed to observe the effects of resistive switching by different polarities on the samples. The polarity of applied voltages is known to have effects on operation and behaviour of the samples. Our memristor MIM MgO structured samples are voltage controlled. The applied voltage began with voltage sweeps under '+' bias, then '-', followed by a '+-'and '-+' . This is referred to as our voltage scheme. A depiction of the obtained hysteresis loops showing memristive behaviour is shown in figure 18 a) and b). Switching ability under all the voltage bias schemes was seen in the devices that experience resistive switching and hence all devices had reproducibility of switching cycles under this voltage scheme.

Beginning with the test sample 'S2', electroforming was performed using an applied positive voltage bias for consistency on numerous samples. The electroforming process is considered a SET and occurred by applying a gradual increasing voltage from 0.05V to 12V in increment steps until an abrupt change in current appeared. Then a lowered sweep voltage to approximately 9V is applied for subsequent SETs. For one of the devices as

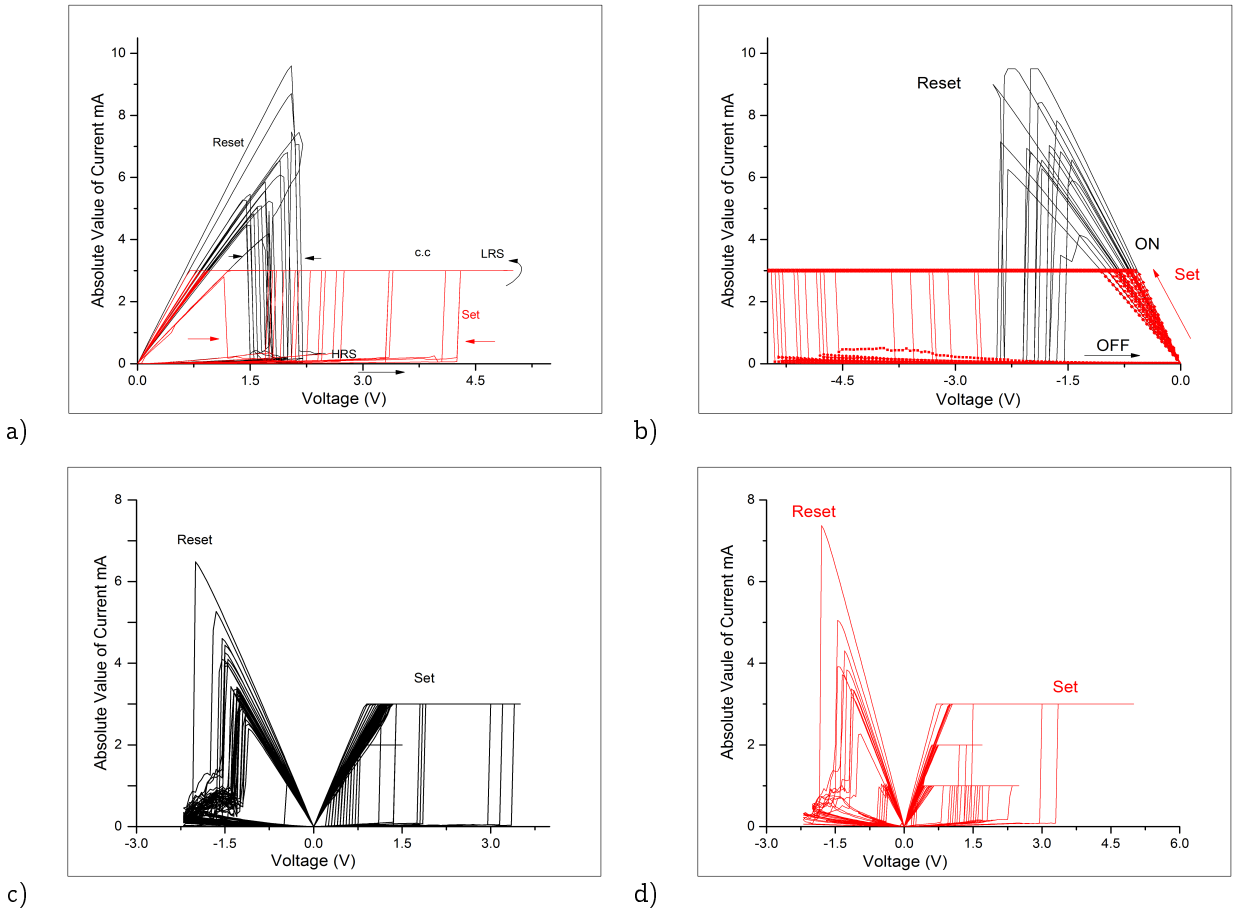


Figure 18: A depiction of the voltage bias scheme applied in order from a) to d) to the samples. In a) represents '+' bias, b) '-' bias, c) '+-' bias and d) '-+' bias.

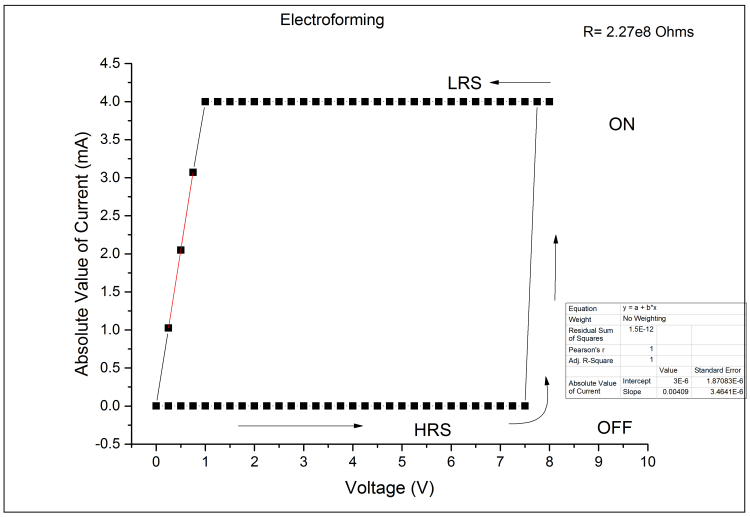


Figure 19: The electroforming step performed under positive bias. The inset shows the slope of the curve for resistance value from a LRS to a HRS. The initial HRS at 0.5V is 2.27e8. In this device a high c.c was chosen but subsequent to this much lower values were chosen.

shown in the figure below the device goes to an ON state at an initial voltage of 7.75V for a high resistive state of 2.27 x 10 ^8 Ω at 0.5V and then decreases to 244Ω in its ON state. Comparing to the SETs shown prior this forming step has a higher voltage by a factor of 2. The current is kept at a constant for 4mA as the current compliance. The electroforming step is prominent in metal oxides and is a result of internal electro-reduction of oxygen ions or metal ions in the MgO under electrical stress. This step was also performed with a negative bias. In samples to follow it was realize that a smaller current compliance was better for switching results. Current compliance is known to be directly related to the shape of the conductive filament [2].

A controlled approach was taken to study the IV characteristics of the sample by defining the administered voltages to a scheme. Firstly the forming was always performed by a positive bias, with the top electrode of Ta/Ru having the positive probe attached and the Pt to the negative probe. A scheme to test the sample performance by reliability of 50 plus cycles for different biases followed. The electroforming process is related to filamentary switching, it is irreversible, where an established conductive filament provides conduction through a dielectric but also induces more defects in the material.
Resistive switching is a special type of electrical switching experienced in memristors. Particularly, resistive switching can be classed by two schemes either as unipolar or bipolar. It is observed for this MgO memristor sample the scheme was unipolar. The reason being is that the SET and RESET are not dependent upon the change of polarity of its input but the applied amplitude of the input. The voltage sweep spanned from 0V-6V and there was reproducibility of SETs and RESETs.

The SET and RESET operation pertain to the formation of a conductive filament and its dissolution within the dielectric under the action of electrical stress. They correspond to the device being switched ON or OFF respectively. In figure 20 the SETs are shown in red and range to approximately 4.5V. The SET process is formed by an abrupt increase in current of 0v to 3mA at particular voltages. A reason for SETs occurring at different voltages may lie within the conductive path; several conduction channels may have arisen in the oxide

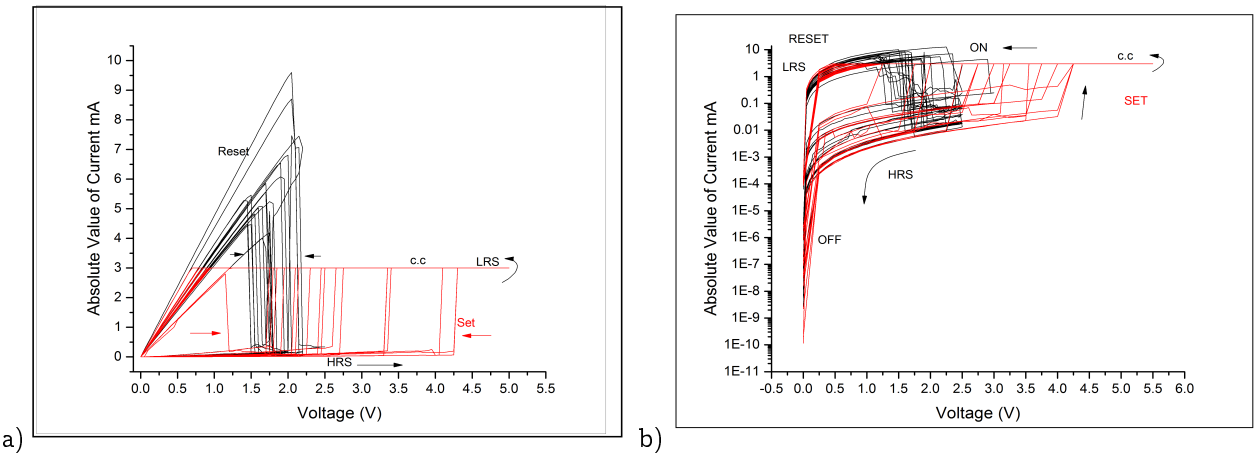
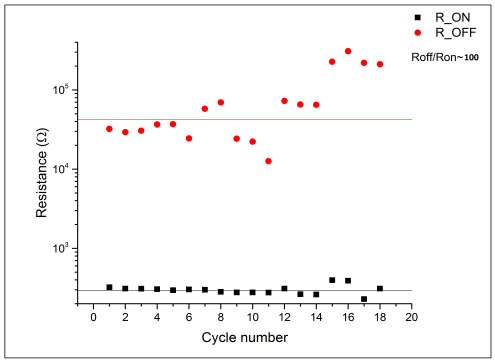
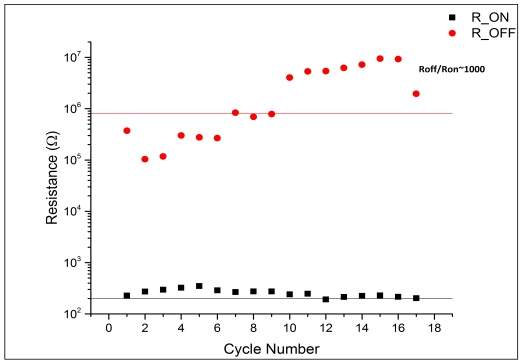


Figure 20: Showing the switching of SETs and RESETs for a device in sample S2. In figure a) the RESETs are shown in black and the SETs in highlighted in red, with the indicated current compliance (c.c). In figure b) shows the same graph but in a logarithmic form for the current.

[28]. While the RESETs shown in black range to 2.5V, between a current of 0mA to 10mA, adverse to the SET is an abrupt decrease in current at a particular voltage. The RESETs exhibit higher levels of current, as they required more energy to break the conduction filament formed by localized joule heating. Depending on the shape of the conductive filament, the RESET graph would require a particular voltage [50, 6]. Numerous SETs and RESETs processes were achieved by continuous voltage sweeps within 100ms of each other. After each sweep there was a comprehensive amount of switching that showed hysteresis behaviour. Voltages were applied as positive, positive-negative, negative- positive and negative biases through electrical contacts, since switching can be modified by bias application [6].Though larger input voltages were administered to the device as seen in the SET process in 20 a), the device performed a SET only based on the energy it needed to create a bridge between one electrode to another. The rest of the energy is discharged in the sample as excess heat [38]. Since the voltage needed always varied, one SET voltage could not be determined to configure repeated SETs forming. This behaviour confirms what is known of resistive switching devices. A similar aspect is seen in the RESET operation. RESET voltages seem to congregate around a narrower range. This can be explained by the second law of thermodynamics. Beginning with the creation of the conduction path, the closed system has entropy. During a reversible process the system remains unchanged, requiring less energy to break or disrupt the conduction path. This is seen in the lower levels of voltage needed for the RESET process across the sample. A higher level of current is shown in the figures for RESETs. These current values are shown in the figure to span from 4mA-9.5mA; and is the amount of charge needed to flow through the conductive filament to cause enough joule heating. Eventually this heat will disrupt the conduction path and return the device to an OFF state but not its' initial OFF state. The RESET process strongly correlates to the SET process. The mean RESET current was found to be 5mA in relation to the mean of the SET processes of 2.3V. The mechanism which drives the conduction between the electrodes can have a number of origins. One of them is the relation between the electrodes and dielectric interface. The device can possibly switch ON or OFF at the interface of one of the electrode and dielectric. In this case, Pt and Ta electrodes were used, with electrical contacts being made using tungsten micro-probes. The Ta electrode served as the active electrode and Pt as the inert electrode. The conductivity through the dielectric MgO is made through hopping conduction by ionic movements possibly that of oxygen ions due to higher ion mobility in HRS state and had a space charge



a)



b)

Figure 21: Comparison of resistance ratios under positive and negative applied voltage biases for a device in sample S2. In both cases a) and b) there is a clear distinction between the two states.

limited conduction mechanism (SCLC) and ohmic conduction between in LRS. There is also the presence of Schottky effects and Frenkel defects which create low resistance pathways within the MgO thin film [8]. To initiate the succession of SETs to RESETs, an electroforming process was observed for MgO memory device

7.1.3 Analysis of Sample S2 of 30nm

The graphical depiction of the behaviour of sample 'S2' shows resistive switching behaviour for positive and negative biases. Sample 'S2' showed the highest level of working devices and had a substantial number of high initial resistance states for its devices.

Resistance Roff/Ron ratio: A plot for Roff/Ron resistances was made under large cycle number. A clear distinction is seen in both figures 21 a) and b), leading to a conclusion that ON/OFF states is clearly distinguishable in the sample. In the positive voltage bias in 21 a), the Roff/Ron ratio is ~100 whereas for the applied negative voltage bias in 21 b) shows Roff/Ron~1000. The progression of switching cycles indicate that uder a negative bias the HRS becomes more stable. Under both biases of positive and negative there is no degradation of resistive states. A clear distinction of resistive states allows for the identification of signal-to-noise ratio in memory devices action[49].
Another factor influencing the resistance states is the current. The current applied for the SET process is controlled and constant, whereas the current in the RESET process is an effect of experimental influence. Observing the Ireset versus Ron curve shown in figure 22, it is seen that with an increase in current of 5mA there is a larger number of low ON resistance states between 300 -400 ohms. Ireset decreases linearly with Ron for the MgO . This is an expected result as a higher level of current implies a greater flow of ions through the sample by an increase in the conductive filament diameter. Since the MgO memory device experiences unipolar switching, the conductive filament disruption is directly related to Ireset versus Ron [2].

Delay Time: The sample was tested to see the effect between the cycles for time intervals for a repetition of a SET and RESET. A timing range began at 10s to 60s interval was considered as shown in figure 23 a) and b) respectively. The study of long delay times above 10secs range, showed a reduced number of SETs

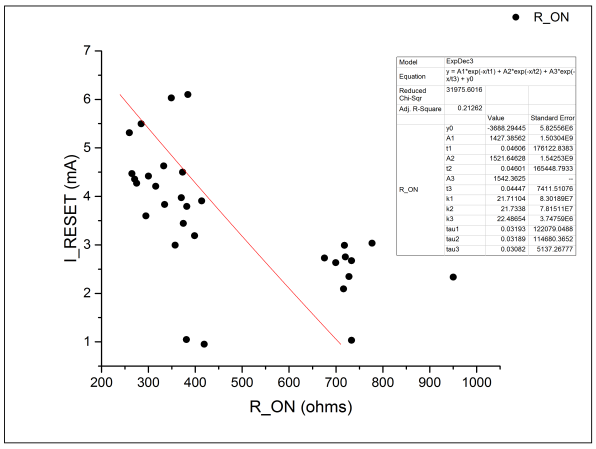
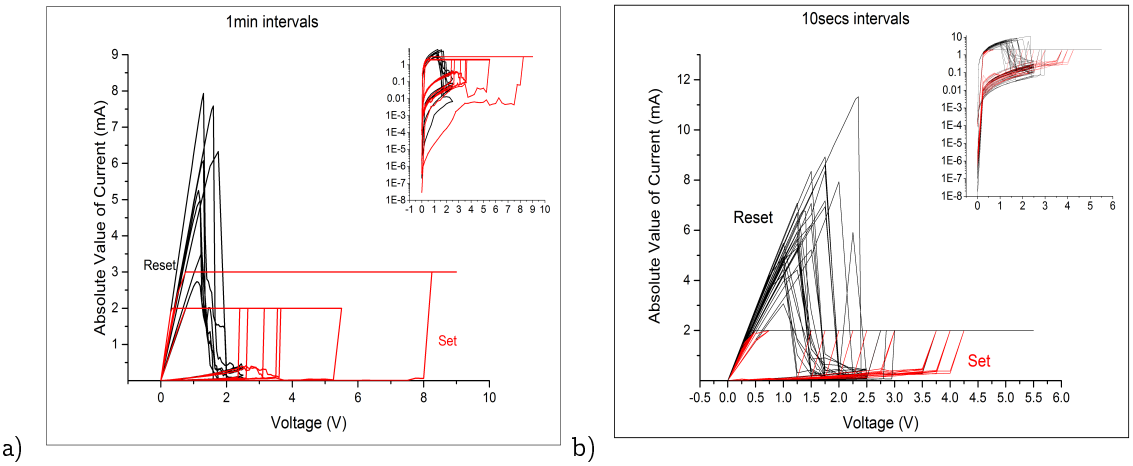


Figure 22: Showing for a device in sample S2 the Ireset current vs Ron. As shown the higher ON resistance states occur at lower reset currents.



a) b)

Figure 23: Time delay studies on MgO sample F for different polarities. In a) the positive bias for 1min intervals between SETs and RESETs is compared to b) for 10sec intervals.

and RESETs processes being formed as seen in the figure 23. There is an apparent higher SET voltage of 8V needed to perform a switching cycle as compared to the 10secs figure 23 b) with its maximum SET voltage at 4V. Delay times of 10secs showed a higher number of SETs and RESETs achieved overall under different voltage bias schemes. It can be inferred that by shortening the time delays significantly can lead to an increase in the switching dynamics. Typical resistive switching memory devices or ReRAM devices are known for fast switching speeds within a nanosecond range [28] where effects of read and write operations are seen. It appeared that switching speed has an effect on the switching voltage, particularly the SET voltages.

Statistical distribution of Switching Parameters of sample S2: Metal-Insulator-Metal (MIM) ReRAM devices are known to exhibit high variability in voltage parameters for device operation [4]. This was also observed for the MgO memory device. The goal would be to achieve a single value of voltage and current that will always give a SET or RESET process. This will make the device reliable and partly controllable for practical uses. To study the switching parameters dynamics, a python program was used to show the

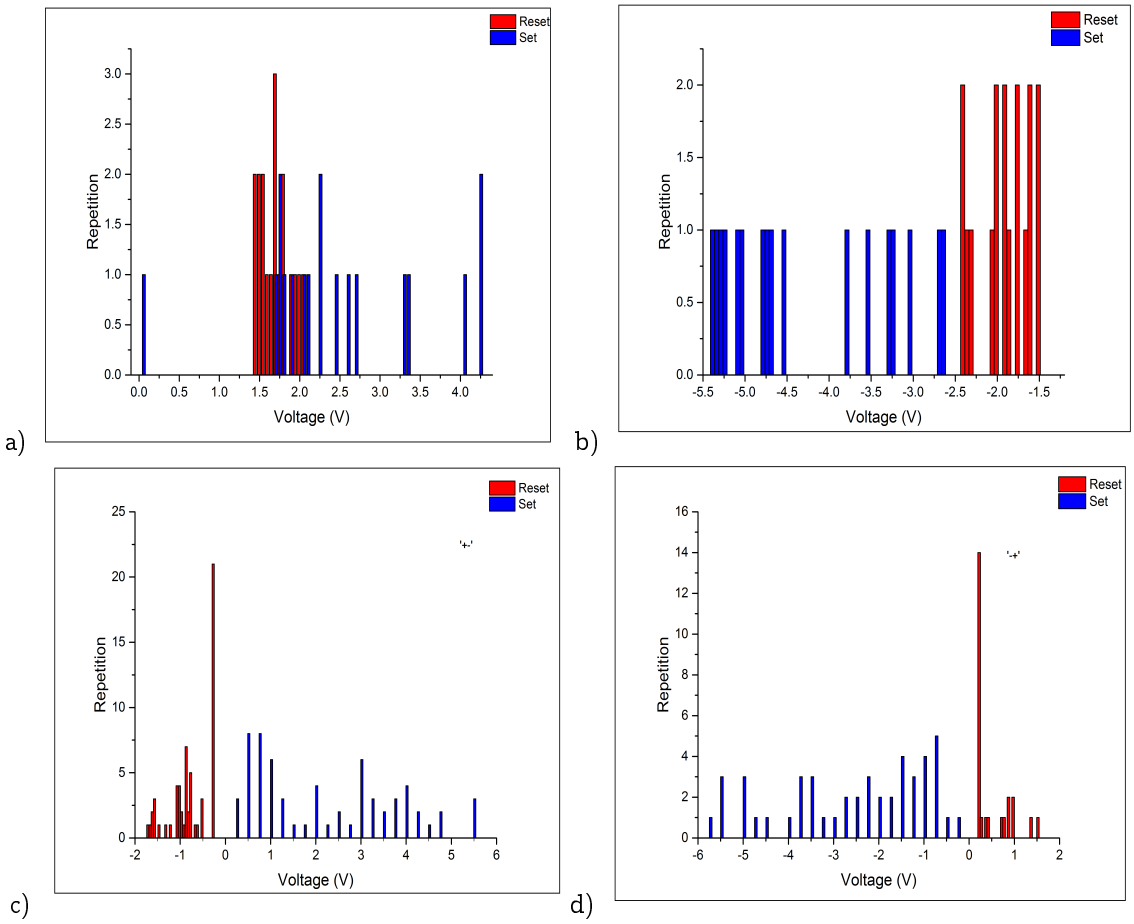


Figure 24: In figures a) and b) shows the positive and negative applied voltage bias respectively. In both figures the SETs are disperesed and span a wider range of voltage values. In contrast to the RESETs that has a narrower range of voltage values. In figures c) and d) shows the ' -+' and '+-'.

I/V characteristics of SETs and RESETs of the sample. In sample 'S2' the observed variability is as shown in the figure 24. A voltage scheme of '+', '-', -+', and '+-' biases as shown in figure 24 a), b), c) and d) respectively, was applied to reach 50 or more cycles for the chosen device. A comparison of the bar plots indicates that RESETs tend to have a narrower range as compared to SET operations that have a wider span for voltages. In the positive distribution the RESET ranges between 1.5V to 2V for a total of 18 SETs and RESETs. There exists some overlap in voltage values of SETs and RESETs ranging from 1.5V to 2V. The cycle number achieved is based upon the administered parameters for voltage and current, here the voltage ranged up to 5V for SETS and 2.5V for RESETs to ensure continuous switching. The current for the SET is kept at a constant value, to avoid the sample experiencing a permanent dielectric breakdown, which leaves the device in an ON state. A current compliance 3mA was used as this safety parameter. In the negative bias scheme, the distribution for SETs is slightly more condensed as compared to the positive bias scheme. The RESETs maintained their narrow range of voltage values.

With a '+-' and '-+' in 24 c) and d) voltage scheme more impressive results regarding RESETs were obtained. A higher number of RESETs repetition showed to have a constant voltage value. The RESETs also became slightly narrower in the range of voltage values. While the opposite was seen in the SETs voltage values The

Sample	Bottom Electrode		Oxide	Top Electrode			
S1	Pt	SiO/Si/SiO/Ti	MgO 15nm	Ta	200	Ru	50
S2	Pt	SiO/Si/SiO/Ti	MgO 30nm	Ta	200	Ru	50
S3	Pt	SiO/Si/SiO/Ti	MgO 22.5nm	Ta	200	Ru	50
S4	Pt	SiO/Si/SiO/Ti	MgO 40nm	Ta	200	Ru	50

Figure 25: MIM MgO sample table

SETs in these schemes showed less repetition for a constant voltage value. It appeared that RESETs processes are controlled by the change of polarity and voltage schemes. Better results overall were achieved for the negative RESETs and positives SETs. One method to understand the wide distribution of varied voltages for the device is the MgO thin film dielectric conduction mechanism. In the pristine state there exist a wide range of defects. These defects are oxygen vacancies, grain boundary, metallic defects and dislocations [42]. It is postulated that the defects are electrically active and affect the electrical conduction through the oxide.

7.2 Comparison of sample S2 with other samples

Sample S2 was the initial test sample to under I/V testing. It was later followed by sample S1, S3 and S4 as seen in the figure 25. Each of these samples has a different thickness of thin film MgO but the structure remains the same. The factors that were applied in S2 remained the same.

S1 The electroforming was performed under positive bias up to 14.5V. It was realized SET-RESET process showed a large disparity in current values. Also applying many input voltage values seemed to have little effect on the sample to induce any noticeable changes through a conductive filament. Instead the sample remain mostly in an OFF state. It was observed that the ON-OFF states became progressively closer together for SETs. After a short period of time the device remained on the ON state. In particular, one device of sample S1 only one SET-RESET cycle was achieved largely separated. The conclusion is that the sample current compliance (c.c) is too large for the electroforming process and it is suspect that due to the smaller thickness of this sample, there was no electroforming process. The current compliance (c.c) is directly related to the conductive filament diameter [2] . As seen in the figure 26), with such a large current compliance the conductive filament diameter would be more difficult to rupture.

S3 The electroforming was performed for a positive bias and under this initial condition for one device showed there was an accomplished total of 45 SETs and 41 RESETS. Observing specifically the positive bias statistical distribution shown in figure 27 a) and b) of SETs and RESETS, there is a smaller voltage range as compared to sample S2 at 0.25V to approximately 3.65V. The forming voltage occurred at 11.25V for 1mA c.c. It is known even at this forming current compliance (c.c.) the conductive filament diameter is large; hence one would expect that the first SET voltage would be high. There is an average SET voltage of 1.67V and the RESET at 1V. As the testing continued the device behaviour began to slightly. It became noticeable

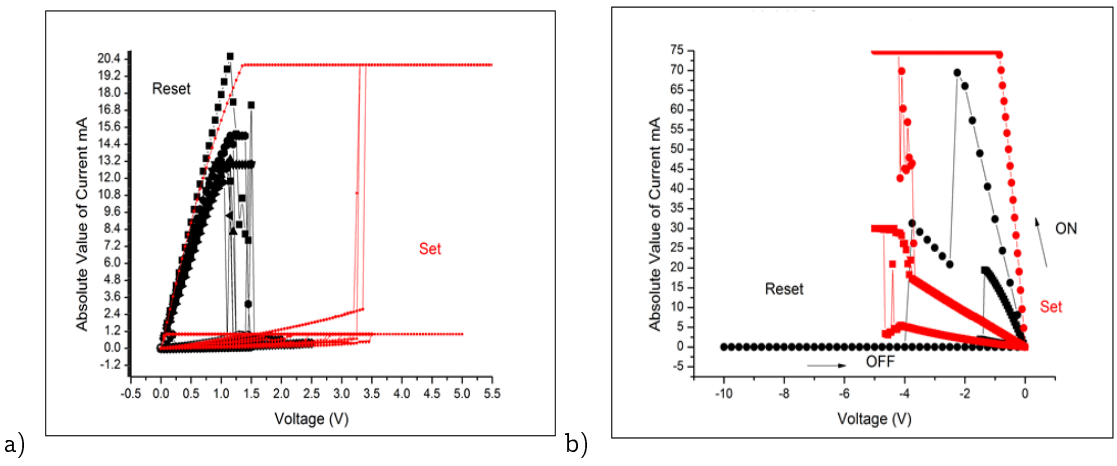


Figure 26: Showing the positive cycles of SETs and RESETs obtained in a) and the negative cycles in b) Very few repetitions was achieved before the device went to an ON state.

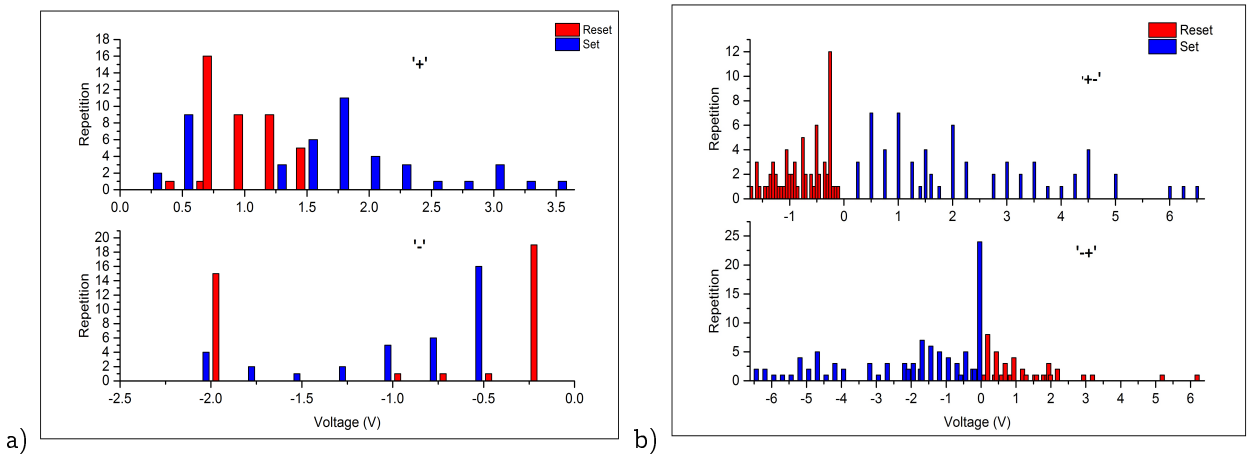


Figure 27: The following distributions show the entire voltage scheme was achieved for a)'+', '-', b) '+-', and '-+'. The negative scheme shows that the voltage range is much narrower as compared to the others and closer for the SETs to RESETs. Overall the single positive and negative biases gave the best results, for less variability in SETs and RESETs voltages. The resistance states are not as distinguishable as seen before.

that as the cycle number increased the SET voltage disparity enlargen as compared with the RESET voltages. The RESET voltages showed less variability as the cycles increased. These average voltage values are higher than the previous S2 sample. The resistance state for this sample range from average ROFF 1.03e+05 ohms/ average RON2.36e+03 ohms. A smaller ratio between Roff/Ron is seen.

S4 The forming voltage occurred at 8.25V at 1mA. For the sample S4 overall there were a higher forming voltages than other two samples S2 and S3. The SETs and RESETs voltage distribution indicates that the negative cycle SET and RESET shows less variability as compared to the other bias schemes. It is apparent as compared to samples S2 and S3, S4 had the largest SET voltage achieved. The device quickly turned to an ON state during the last voltage scheme of '-+'. During this bias scheme one of the highest RESET voltages was seen at -3.75V. Within all the voltage schemes there exist two major peaks representing the highest repetition

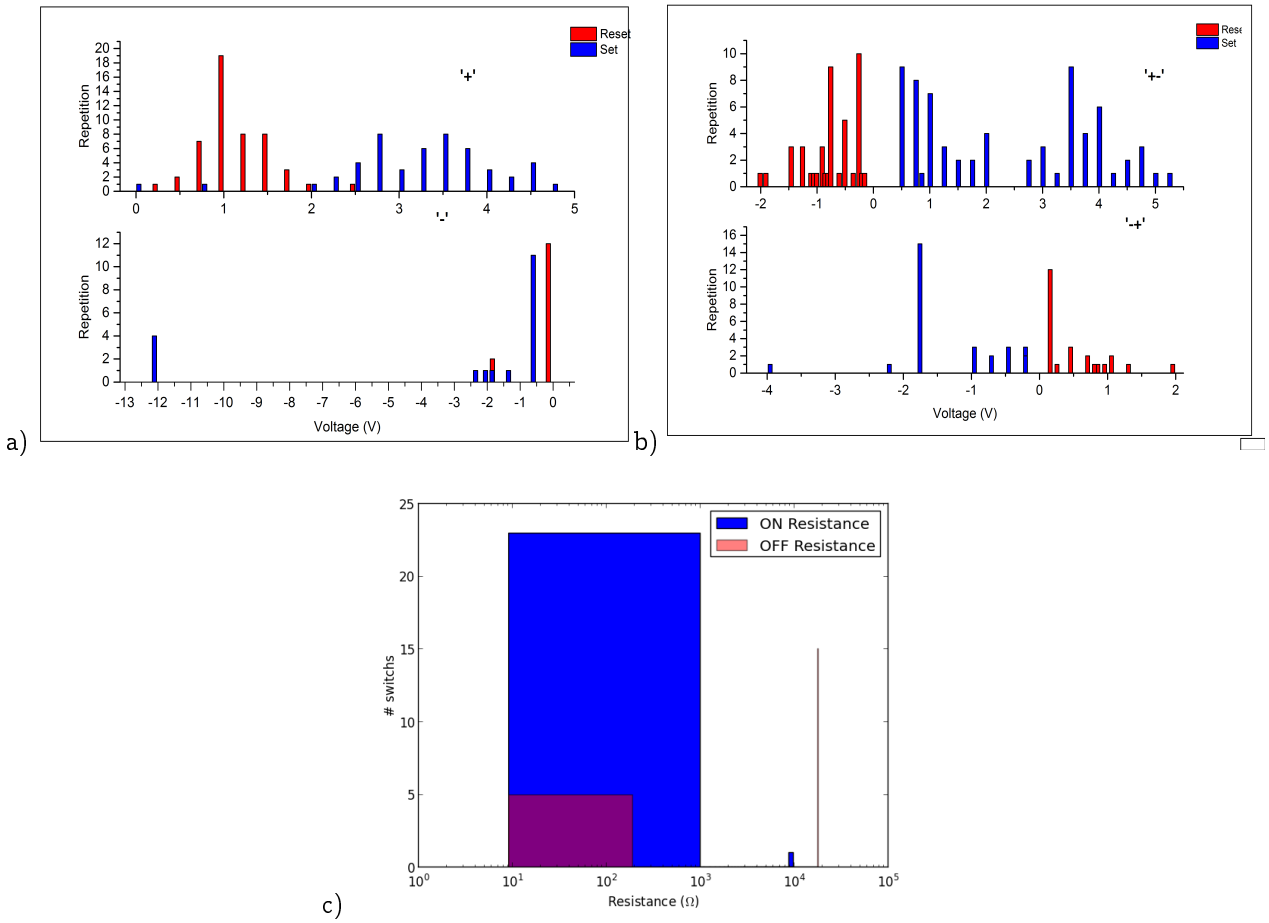


Figure 28: Showing the statistical distribution of SET and RESETs voltages in a) and b) . In c) the OFF/ON resistance ratio of the sample S4.

values. This is a possible bimodal distribution; which appears most prominent in the '+-' scheme shown in figure 28. As the cycle number increase, the I/V characteristics changed and appeared more plateau. This was observed for SET and RESET voltages that appeared to fluctuate less, and resistance states ratio were not clearly distinguishable before the device went to an ON state. Overall this sample did not have much working devices that reached 200+ cycles.

Device Performance Studies The ability of a device to switch efficiently between SETs and RESETs would make ReRAM devices as or more reliable than its counterparts. To ensure this occurs, a large number of working cycles from SET to RESET repetitions would be needed for a particular device. Two of the samples, S3 and S4 were selected to be tested. Working devices were tested until they reached their maximum for switching and they can no longer obtain a SET or RESET under any chosen I/V parameter. A device for a Sample S3 showed a high endurance of over 340 working cycles in 29 b) under a positive bias. Its average SET voltage was 3.62V, and RESET voltage 1.24V. The chosen I/V parameters were 1mA, 6V for the SET and the RESET for 20mA, 2.5V. This was similar to all the devices tested and similar in accordance to different samples. The resistance states were clearly defined as seen in the figure 29 a), for an average Roff/Ron of (1.26e5/204). The figure 29 c) for Ireset current versus Ron resistance showed similar results to sample S2,

with an overall increase in current to low ON state resistances. An attempt to achieve similar results for the sample S4 proved not as successful. There was an average of 120 working cycles for the devices of S4.
A table summarizing the comparison of the I/V characteristic is shown in the table 1. It is seen that sample S2 shows the least variation in average SET voltage when compared to the devices of samples S3 and S4. The RESETs in all samples showed little variation between each other, this can indicate some similarities in device to device stoichiometry, since the behaviour of the RESET is induced internally by the nature of the device and not the experimenter. Sample S2 also had the better resistance ratio for Roff/Ron giving distinct binary states for OFF-ON or '1' to '0'. Throughout I/V testing sample S2 outperformed the other samples, in SET/RESET cycles, working devices and resistance ratios.

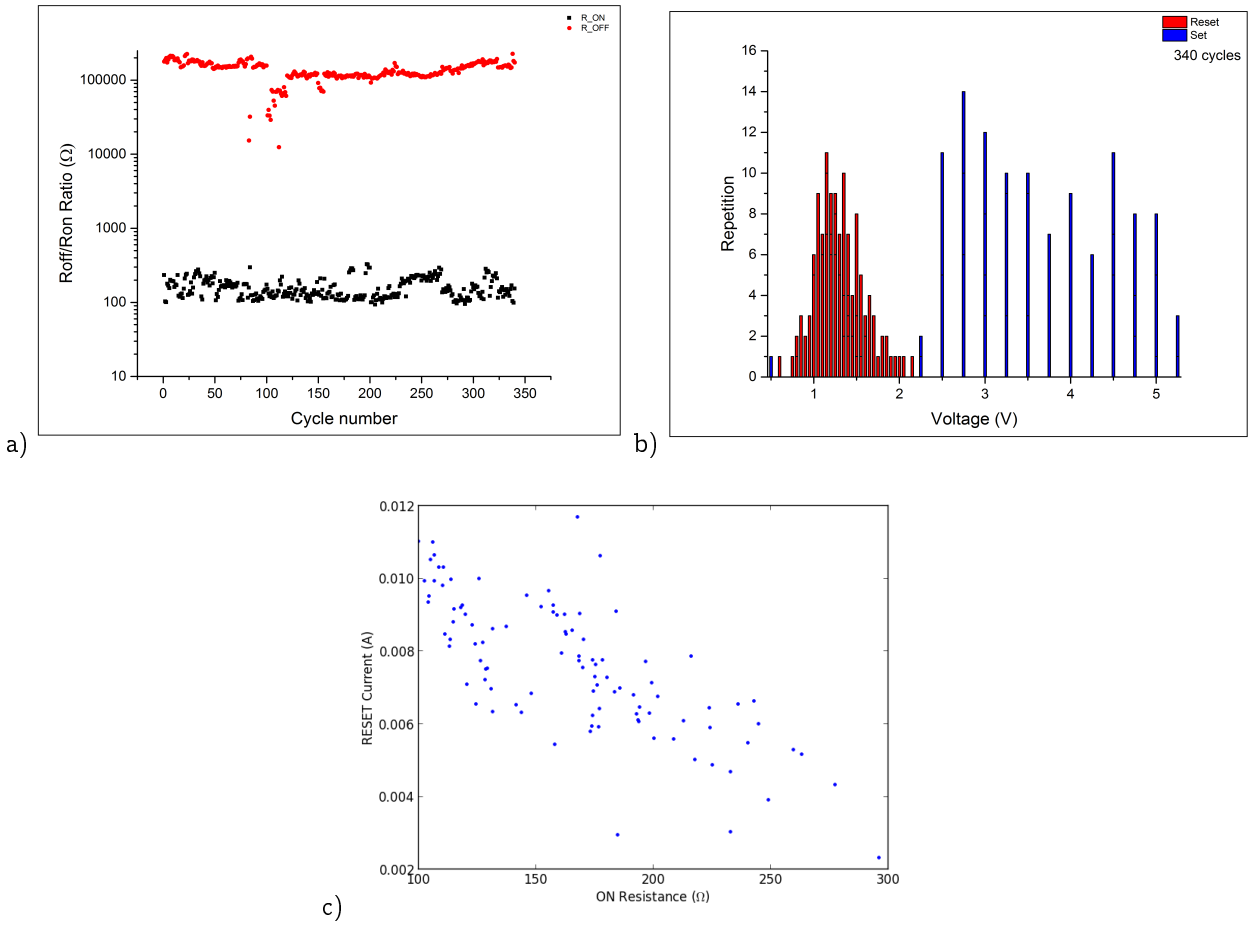


Figure 29: The performance of a device in sample S3 shows resistance states in a), b) the statistical switching dynamics of SETs and RESETS and in c) the Ireset versus ON Resistance.

Sample	S2				S3				S4			
Voltage Bias	Average Set/V	Average Reset/V	Roff/ohms	Ron/ohms	Average Set/V	Average Reset/V	Roff/ohms	Ron/ohms	Average Set/V	Average Reset/V	Roff/ohms	Ron/ohms
+	2.26	1.4	1.17e+06	1.13e+06	1.62	1.0	1.03e+05	2.36e+03	3.3	1.15	4.73e+06	435
-	-4.9	-0.85	1.55e+03	9.9e+03	-1.25	-0.09	491	250	-3.19	-0.49	921	272
+-	2.23	-0.75	2.28e+05	3.69e+04	2.24	-0.76	1e+08	6.19e+05	2.36	-0.74	1.78e+04	3.99e+03
-+	-2.59	0.52	3.07e+04	1.27e+03	-2.05	1.32	2.15e+08	-2.35e+08	-1.35	0.04	7.39e+03	2.62e+03

Table 1: The table depicts a device chosen at random on a selected sample. The sample with the most working devices was sample S2. One of its devices shown here has the closets SET voltages and RESETs and the most distinguishable Roff/Ron ratios.

Post testing Effects The I/V tests were perform using tungsten micro-probes on the devices for the samples. The positive bias is always applied to the top electrode and the negative bias at the bottom electrode. This external factor causes a change in the behaviour of the device from its pristine state. The electrodes act as a boundary to the dielectric sandwiched inside, typical for MIM structures. The majority of the changes occurring in the device takes places inside or near the dielectric, which used here is the MgO. It has been reported by Huang in their sample that Mg+ ions mobility is repsonisible for conduction, it has also been said that the oxygen ions posses a higher ionic mobility. One way of knowing which ions were mobile in our samples was to observe the topology changes after I/V testing using a optical microscope. This is shown here in the figure 30.

It is noticeable from the picture fractures that appear in a) to d) to be circular or 'bubble-like' in nature and are sporadic are dispensed across the surface of the devices. There is some refraction of light under the bright field in 30 a) and c), displaying varied colours. This indicates an exposure of a metal. This is confirmed by the dark field pictures. As oxygen ions are reported to be highly mobile these pictures can indicate the favoring of oxygen as the mobile ions in our samples. In sample S4 some of the devices figures 30 e) and f), there was the appearance of 'lattice trees' structures on the surface of the sample after testing. This could be the possibility of the bottom electrode appearing due to a fault in the fabrication process.

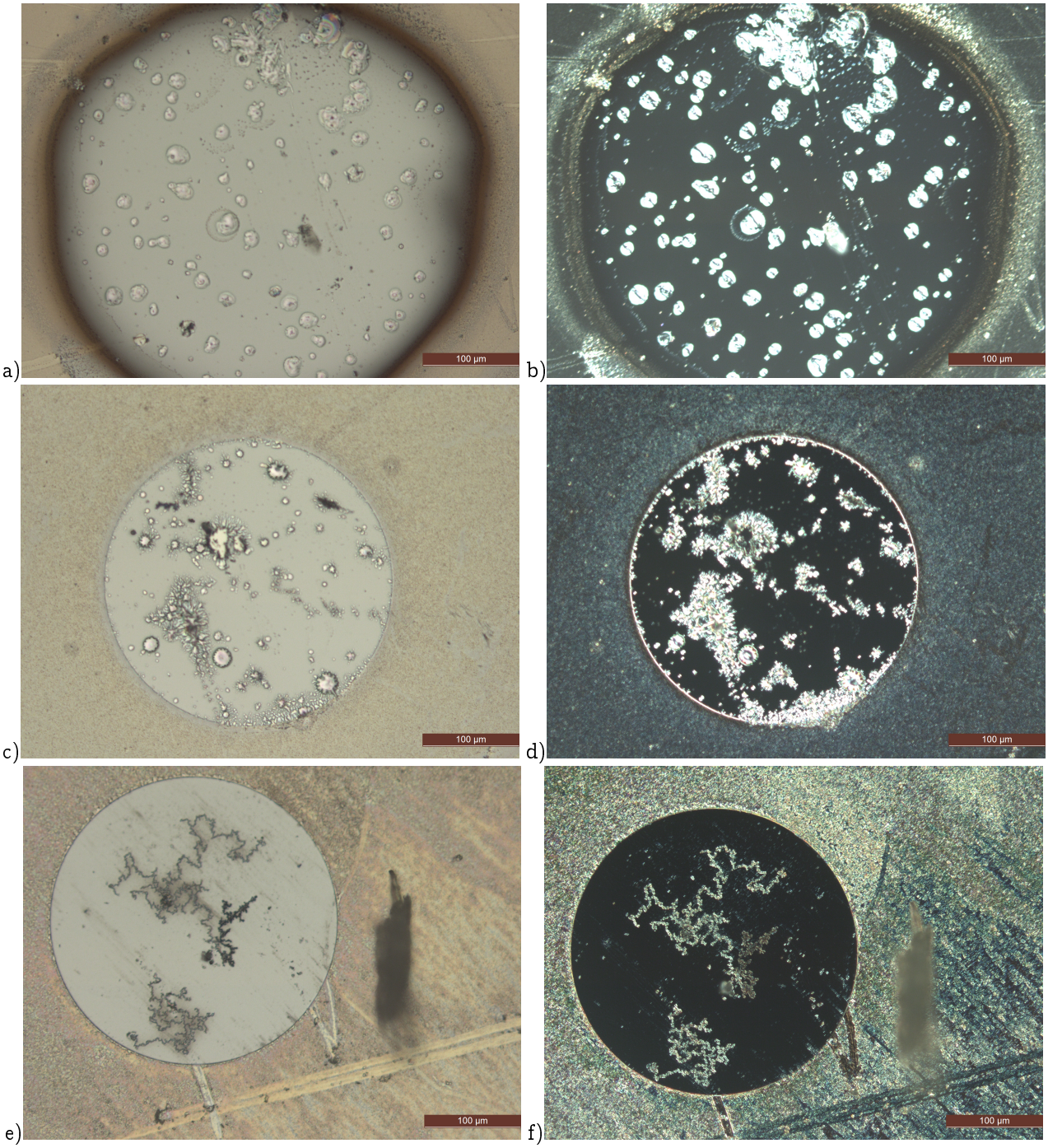


Figure 30: For samples S2,S3 and S4 respectively a) to d) shows the post testing topography of devices on both samples. In a), c) and e) shows pictures taken with an optical microscope for a zoom of 20x under bright field and b), d) and f) shows pictures taken for a dark field.

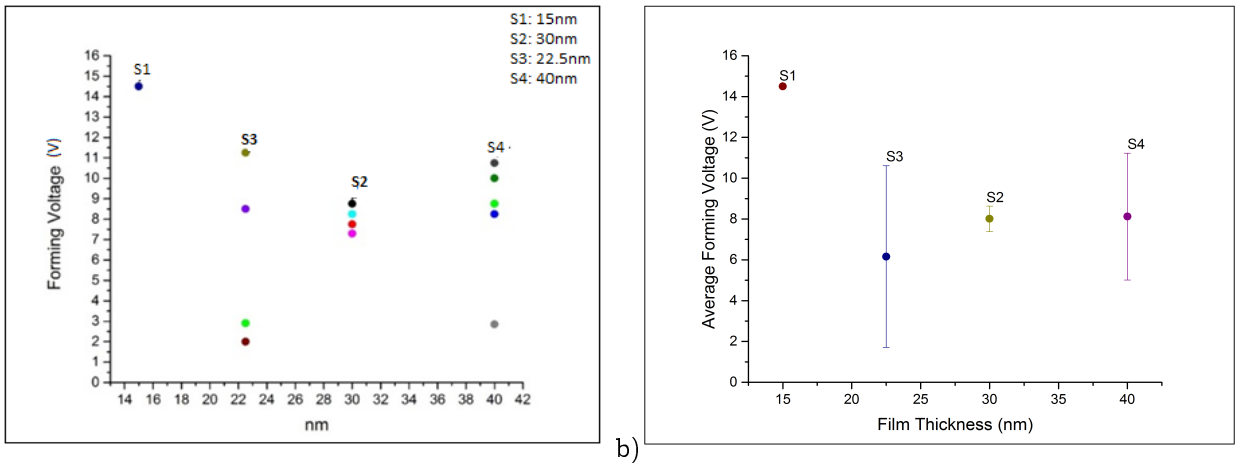
7.2.1 Conclusion

To achieve conductivity in the MgO thin film one needed to establish a near or soft dielectric breakdown. This was accomplished by applying an electrical bias to the system. Once identified as a memristor and as a resistive switching device, our memristive device was voltage-controlled. In resistive switching, when a dc voltage bias is applied initially in a large quantity it can achieve a soft-dielectric breakdown to initiate the first SET process known as the electroforming step. In the four samples of S1 and S2, S3, and S4, MgO thin film thickness was varied. Initially a low current compliance was applied at 1mA with an ever increasing higher voltage from 2V. The electroforming process was down in the following figures for cycles "+ or-"biases, but the chosen positive bias was decided upon. The electroforming SET process was noticed to be larger than mostly all of the following Sets and Resets in succession. Graphical analysis was performed on all samples to show the resistive switching from an ON state to an OFF state consecutively. Observing the graphs it was seen that RESETs were obtained for a higher current compliance but also a smaller voltage. The voltages were noticed to be within in a narrow range 0V-2.5V average for all the samples with a few outliers. The RESETs voltages showed less deviation from their norm after sometime as compared to the SETs voltages. The average SET voltages range went spanned from 0V-5V. This range was irrespective of bias polarity. In conclusion the SETs and RESETs behave differently and this is also synonymous with devices in one sample. Each device has its own specific parameters for obtaining switching which is related to the stoichiometry of the device.

7.3 Oxide thickness dependence on resistive switching

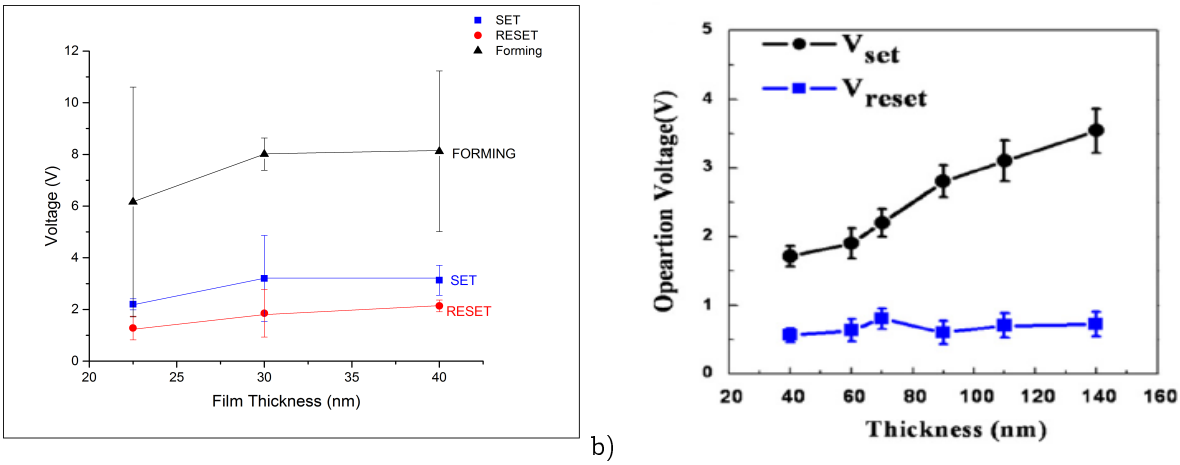
Under a comprehensive examination of the I-V characteristics distinguishable resistive switching behaviors was observed in the magnesium-oxide memory devices for the different thicknesses. Each sample was subjected to the same initial conditions of 1mA which beget testing and the parameters for electroforming and resistance in relation to the MgO thin film thickness were studied.
On each device conditions were imposed to cause a soft dielectric breakdown in the oxide layer by varying the current and the voltage from low values of 0.001mA-1mA and 1V and above until the device moved from a high resistive state HRS to a low resistive state LRS. This process is referred to as the electroforming and is shown by the forming voltage, a condition for the first SET process. The different thicknesses of MgO were checked by the forming voltage as shown in the figure 31 a) by making positive bias voltage sweeps. The initial thickness of MgO of 15nm labelled as S1 had the highest forming voltage of 14.5V but had only one repetition of SET to RESET switching before experiencing a full dielectric breakdown. The device permanently stayed in a LRS. The second sample labeled S3 at 22.5nm shown in the figure 31 a) displays a dispersion of forming voltages.
The study of I/V characteristics revealed that the various samples behaved differently under the same controlled conditions. An important factor revealed that one of the conditions for change was the samples thickness. The different thicknesses of MgO was examined by the forming voltage as presented in the figure 31 a) and b), by making positive bias voltage sweeps. In previous studies forming voltages were undertaken with a negative voltage bias that showed superior reproducibility of switching cycles as compared to forming performed with a positive voltage bias. In future work this aspect can also be consider for a comparison with the the current positive voltage bais.
The voltage required for the device operation, the forming voltage of SETs is noticeably higher for thicker oxides. In figure 31 b) the average forming voltages from a number of devices for one sample indicated that with increasing thickness the forming voltage also increases. Figure b) implies that the forming voltage has a dependency upon the thickness of the oxide. The I/V characteristic of higher voltages with a comparable HRS region, indicates a Poole-Frenkel emission [8, 51]. The forming voltage for sample S1 of thickness 15nm was at a high of 14.5V and sample S4 of 40nm had an average of 8.12V. The S1 sample had the least amount of working devices as compared to S4. Our MgO thin film is monocrystalline in nature. The crystallinity could possibly be improved with the oxide thickness by the decrease of defects such as grain boundaries and dislocations. The presence of these defects would explain the higher voltages noticed in our S4 sample. Lower forming voltages were seen in samples S2 and S3 with an average at 8.01V and 6.16V respectively. It can be seen in the figure 31 a) that sample S2 displayed the smallest span of forming voltage deviation as compared to the other samples, in particular sample S3.

In figure 32 a) the further relation between SETs and RESETs were considered. Initially the electroforming step showed a directly proportional relation. This relation is also seen with the SETs succeeding the electroforming process. There is a distinction with the RESET process, where ohmic conduction seems to occur. The RESET voltages for the samples show an almost constant relation. Previous experimental work on ZnO:Mn by Yang indicate similar results for forming, SET, and RESET dependence on oxide thickness. The latter is shown as a reference in figure 32b). This indicates a slight similarity between our MgO memory device and that of the author.



a) b)

Figure 31: Illustrates the sample thickness upon voltage dependence. In a) the samples S1 to S4 depict a few chosen devices from each sample with their forming voltage. An average of these results are shown in b) with there error bar.



a) b)

Figure 32: Forming voltages of SETs and RESETS in a) with relation to film thickness, shows an almost linear relation. In b) shows previous experiments for a sample of ZnO:Mn with similar results.

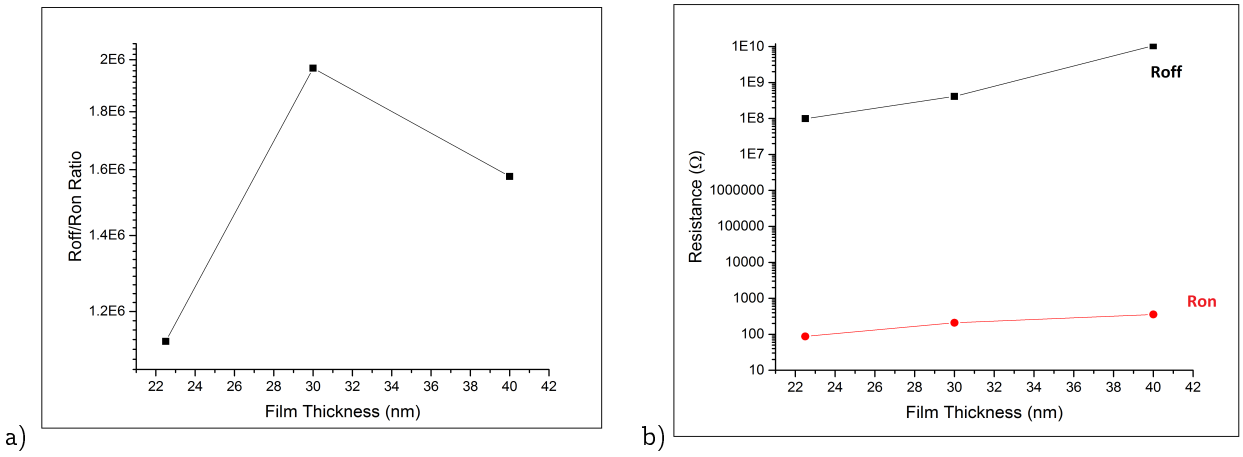


Figure 33: Illustrating the resistance ratio and resistance variance to film thickness.

Figures 33 a) and b) show how the resistance varies with thickness for the samples. The resistance of the different film thickness was measure at 0.5V for HRS and LRS. The figure 33a) shows that from a low thickness of 22.5nm of S3 there is an increase in the resistance to S2 at 30nm and then a rapid decrease in the sample S4.

Figure 33b) shows the relation of HRS to LRS state with the film thickness. It can be observed a growing trend of increasing resistance with film thickness for our MgO memory devices, with the HRS by a magnitude of 2 and the LRS by a magnitude of 1. This suggests that as OFF resistance increases the SET voltages increase with increasing sample thickness. There is a decrease by a magnitude of of 2 for HRS with film thickness. Intuitively it can be inferred that as the film is thinner there are a smaller amount of low resistance pathways for forming.

7.3.1 Conclusion

The SET voltages shows a dependence on MgO thickness layer for samples S3 22.5nm to S4 40nm. The forming and SET processes are near similar in their linear distribution. RESET voltages show less effects if any for increase oxide thickness.

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Part IV
Percolation model

As our memristor device using MgO proved to exhibit resistive switching it now belongs to the class of ReRAM devices. The samples showed extensive switching ability but with variability in the I/V parameters. Distinct criterion for resistive switching remain a challenge in our device. It is a problem inherent of all ReRAM devices, as the resistive switching is the cause of a stochastic process. Memristive modelling is an approach to enable one to better understand the complex switching behaviour.

8 Random Circuit Breaker Network model

One mathematical approach to modelling the behaviour of resistive switching is the percolation bond model. This model can be applied to resistive switching phenomenon that can explain our MgO memory device unipolar resistive switching behaviour. We used the random circuit breaker network (RCB) model that inexplicably considers the reversible dynamical nature of resistive switching devices [45]. The RCB model is a computer simulation of the behaviour of the conductive pathway through an insulator. This form of the percolation model is based upon the use of circuit breakers on dual metastable states. Our adaptation looked at the large variability of switching voltages and their distribution for Forming, SETs and RESETs.
Our RCB model is a python program that begins with assuming that our device transport properties can be assimilated by circuit breakers. The python code is shown in the appendix 1, as a), following here we identify the algorithm upon which the code was written.
We defined the two metastable states by resistance values for ON and OFF states by exclusive switching rules. Our simulation consists of creating open circuits connected in a lattice structure. The lattice is structured to mimic different MgO thin film thickness and the number of defects that vary in the oxide. To create a conductive pathway or percolated path through the oxide, we begin with the rules of making open circuits.
The circuit breakers have two resistance states, a high resistance Roff and a low resistance state Ron. We then apply a condition that Roff > Ron. To create a switch to an open circuit, we employ a voltage change that is applied across the circuit breaker. For the ON state from on to off state; $\triangle v > voff$ whilst the OFF state from off state to on state circuit breaker $\triangle v > von$. This action controls the formation and rupturing of a conductive filament.
Our computer simulations is a similar representation of Chae RCB model. It begins with the sample in its pristine state initially to a state full of defects by a probability from 0%-10%. The simulation is programed to run in this sequence:

1. When an external voltage $v_{ext}$is applied at random to the pristine state of the lattice at a probability x%; calculate the $\triangle v$ for the SET.

2. Tally the total current flowing through the lattice. The simulation is stopped at the current compliance Icomp defined valued.

3. Validate if the following conditions are satisfied:

   Condition A: R=Roff for $\triangle v > voff$

Condition B: R=Ron for $\triangle v > von$

4. If the conditions in step 3 are not met proceed to the next increment step of v_{ext}.

5. If the conditions A or B is met then alter the bond resistance so as

   In condition A R= Roff

   In condition B: R=Ron

6. Loop this sequence from step 1 for the newly defined resistance for multiple iterations, with the condition that the bond with the HRS to LRS state its resistance is not repeated.

The result of this algorithm lead to the simulation producing a conductive pathway from one end of the lattice to another through a multiple of switching circuit breakers. This replicates the forming, SET and RESET processes. All the iterations for the forming and SETs obey a rule of ending at the set Icomp value, since the RESETs are controlled solely by the applied voltage the Ireset current is the effect of the material or lattice. Defining the lattice size is varied to span for varied widths and heights. The input values included varied and controlled terms. For the controlled terms included Roff and Ron. The varied terms in our simulations were Icomp for forming and the Icomp2 for the successive SETs and RESETs, voltages Vmax, Vmin,$\triangle v$, Voff and Von, ratios r, and for adjustment of the lattice size which was an MxN martix.
The RCB model is accurate to simulating the effects in the lattice and provided a picture of why the variability of resisting switching occurred within our samples.

8.1 Simulating the structure of the MgO with defects and constructing the conducting filament

The ReRAM memristive devices using MgO were subjected to a soft dielectric breakdown. Once this process occurred, fractions of the oxides contained low resistance areas. The oxide itself has it owns defects that also contribute to low resistance areas [52]. The latter is taken into account by the inclusion of a range of probability of defects from 0%-10%. It is known in some materials that multiple conductive filaments are formed under electrical stress [4]. Through simulations of these low resistance states, the nature of the behaviour of the MgO oxide is modelled.
An inclination for the behaviour of the oxide can be seen by the distribution of the I/V parameters pertaining to SETs and RESETs. On example is the sample S2 as illustrated in figure 34 a), it depicts the forming with a fixed current compliance of 1mA. This is the soft dielectric breakdown occurring for this device at 8.75V. Previously the forming voltages showed it affects the future operation of the device forming a succession of SETs and RESETs. In particular it showed that with a higher forming voltage the average SETs voltages increased slight The forming voltage is an indication of the conductive filament formation and this behaviour is mimic through the simulations.To simulate the forming voltages correctly for our MgO memory device we had to consider that the forming occurred under different conditions based on the thickness of the oxide. Varying experimentally the thickness also meant varying the number of defects within the layer. Thus to encapsulate this feature, the forming voltages had to experience a different probability of defects by varied dimensions of the lattice structure. Following the simulations of the forming process the other factors to consider were the SETs and RESETs.

The figure 34b) shows the variability of voltage parameters between switching for one of our S2 sample devices. If one were to compare with previously shown S2 results it would appear that the voltage spread is different. The reason for the disparities within the same sample is that each device has its signature behaviour. This further makes predictability in ReRAM devices difficult. It is observed over s span of 70 cycles the SET voltage for the '+-' scheme has higher ratios for forming under lower voltages approximately between 1V. In comparison to RESETs the average voltage lies with the highest repetition is approximately 0.4V. Although the majority of SETs process occur below 3V in the '+-' scheme, setting the simulation to run with a maximum off voltage voff at 3V hinders further switching for a longer device endurance. In the '-+' voltage scheme for 70 cycles the majority of switching occurs over -3 to -0.5V. The RESETs indicate a span from a better ratio for having mosts of RESET process at 0.4V. This is a very low value, which indicates that RESETs are predominately governed by Ireset current over voltages. An inference from this results would mean entering lower RESET voltages than SET voltages into the simulation code would produce similar results. To achieve the wide distribution of voltage values we employ an input for higher probabilities of 5% and above. Lastly the figure 34 c) shows that graphical representation of SETs and RESETs for '+-' scheme for the device. The curves are jagged in nature particularly the RESETs. Since the figure 34c) only shows the first few cycles it is apparent that the SETs have a high voltage spread from the beginning phases. The experimental results paints a picture of the values we can adjust in our simulations.

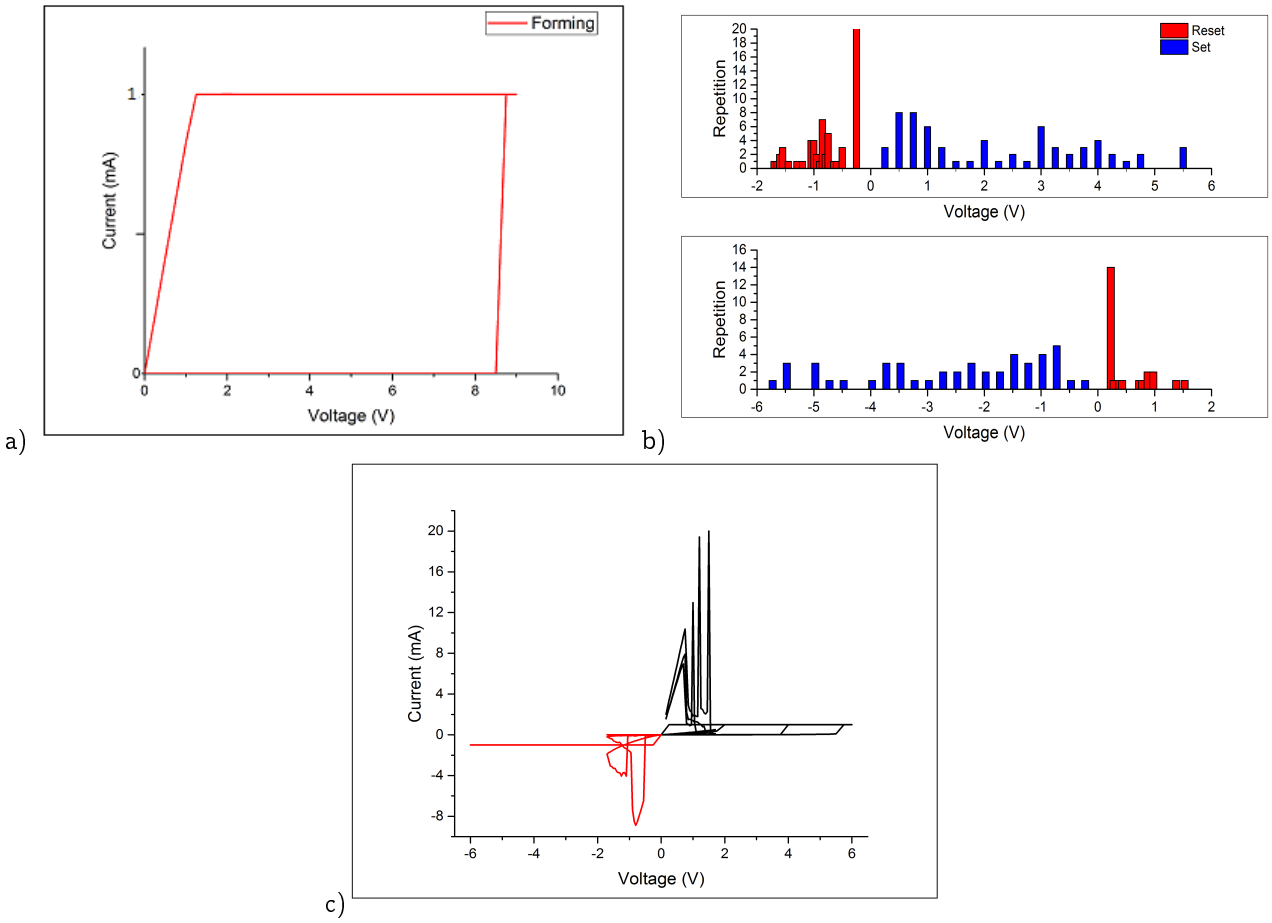


Figure 34: The pristine state of the sample S2 experiencing electroforming is shown in a). The variation of the sample S2 for SETs and RESETs are shown in figure b) while in c) there is represented a few cycles from the '+-' voltage scheme. The maximum obtained SET voltage is 6V but not graphical and depicted in the distribution not all the SET voltages congregate near 6V.

8.2 Experimental Results

8.2.1 Forming

We begun by simulating the forming process. The forming process is crucial as it controls many factor of future switching in the device and device behaviour. Simulating the forming occurred by applying only one Icomp value of 50A into the python program. The resistance remained the same with Roff =1000 and Ron =1. While the voff value was altered. Von was not altered from its set value of 0.2V. The other voltage values of Vmax = 30V, Vmin=0, and $\triangle v = 0.1$. Since prior knowledge led to forming be affected by thickness of the oxide, we proceeded to analyze how forming can be simulated by different lattice size by entering values for an MxN matrix.
The first matrix size had M=20, N=50, the output can be seen in the figure a). The probability of defects ranged from 1%, 5% and 9%. Each of these probabilities had an iteration of running 5x and then the average of the iterations produced the figure in 35 a). The figure 35 a) indicates that the disparity in voltages values for forming is at a 5% defect probability. The largest distribution in forming voltages occurred at 1% probability of the smallest ratio of defects. Since the lattice size represent a thin structure it can be inferred that with a small number of defects the possibility of forming a complete conductive filament is less, and thus a higher voltage is needed. This inference pertains to the size of the lattice and its pristine state. If the probability of defects are increased then the of forming a conductive filament with a smaller voltage increases but there is a limit. If the measure of defects is too large, then there are too many low resistance sites for the voltage to flow, and the voltage becomes dispersed rather than concentrated in the lattice.

Looking inside the lattice is seen in figures 35 b) and c). It shows the different probability of defects inside the lattice for 1% in b) and 9% in 35 c). The computer program has chosen these defects in red at random, which can simulate how a pristine sample of an oxide can look. In the 1% picture, there are very little defects to begin with and a voltage of 2.9V as Voff is needed to create the conductive filament. At this Voff value the conductive filament is formed from initiation to end. A clearer picture of the forming process is observed in figure 35 c). Here the forming voltage Voff is 1.7V and in the first picture of 35 c) we can observe a filament growing in the top left corner by the connection of defects along this path. Then there is an abrupt spark shown in the center picture where the conductive filament is formed. When an external voltage continues to enter the lattice, the conductive filament begins to grow as seen in the last figure. It will grow and spread throughout the lattice until the Icomp is reached. This changes the filament original geometry and as the filament continuous to spread throughout the lattice there will be a complete saturation of conductive pathways. By the continually applying a voltage other structural changes can occur in the lattice structure.

The figure 36) shows a simulation of a 9% probability of defects under the same conditions as before, but with a different forming voltage of Voff = 2.1V. Over the course of time, it appears more than one conductive filament is formed for the same voltage. Another inference that can be made from this example is that time plays an important role in the formation of a conductive filament. As the time increases the conductive filament geometry changes and becomes wider or there can be several conductive filaments formed.
A new matrix size consisting of M= 30 and N =60 represents a slight increase in the lattice size.As seen in the figure a) simulated voltage distribution a slight increase in lattice size increases the forming voltage. Unlike the previous lattice size here Vmax =55V.

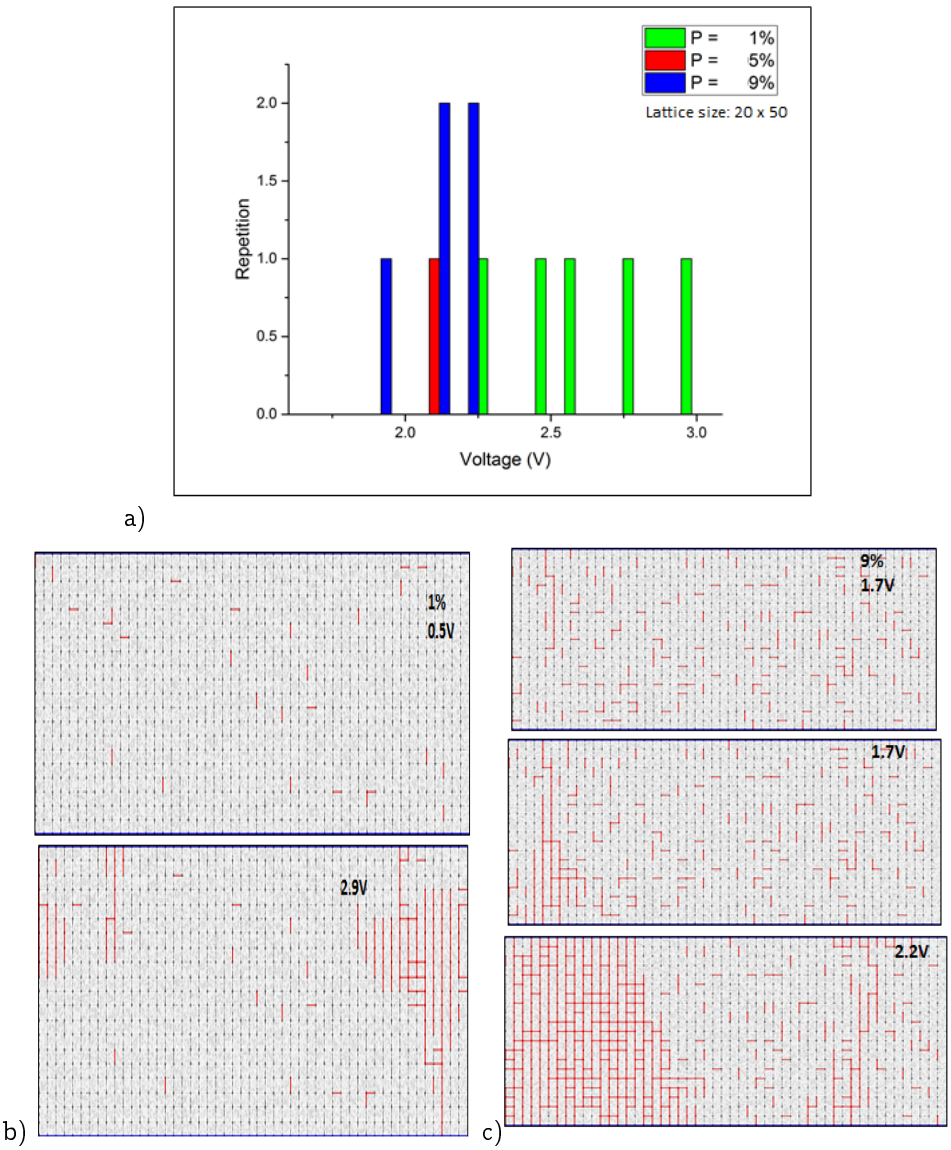


Figure 35: Simulation of the forming process involving a 20 x 50 lattice size. The simulation values were at Vmax = 30V. The distribution is shown how under different forming voltages the disparity between the values are. The lowest disparity is a probability of defects for 5% followed by 9%.

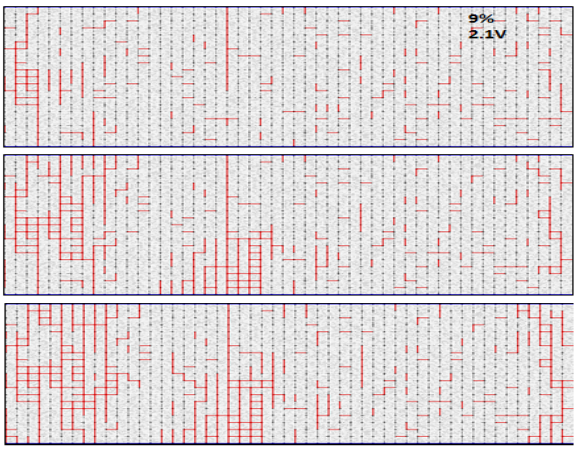
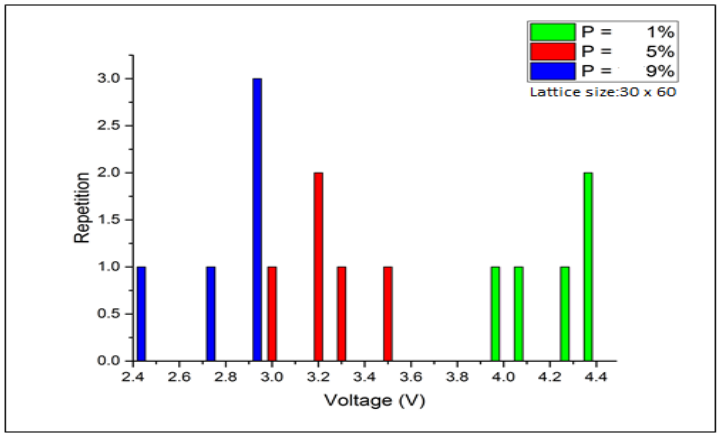


Figure 36: Example of 9% defects for the 20 x 50 lattice structure. Under the same conditions, iterations produce different results. In one of the iterations, roughly 3 conductive filaments are formed for a Voff = 2.1V over the course of time.



a)

Figure 37: Showing the voltage distribution for a lattice size of 30 x 60. The highest probability of defects at 9% gave the least disparity between voltages.

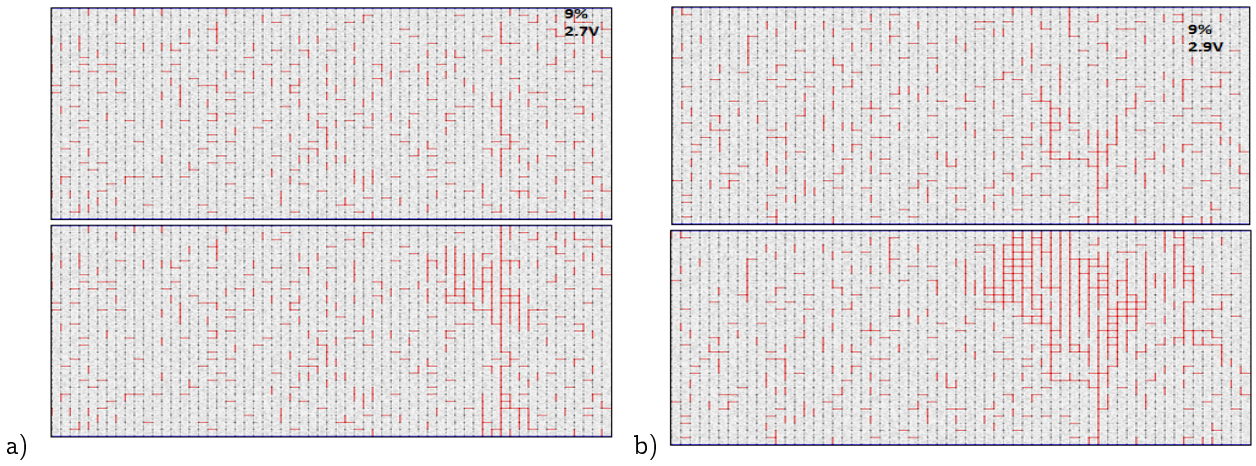


Figure 38: A graphical depiction in a) shows the picture of the conductive filament for a forming voltage of 2.7V with 1 repetition while in b) the the conductive filament is different for a forming voltage of 2.9V with a repetition of 3.

The figure 37 a) shows the same trend of increasing forming voltage with smaller probability of defects. A higher forming voltage influences the device to perform SETs and RESETs at a higher voltage. At the highest probability of defects 9% it is observed that at 3V, gives the highest repetition for forming voltage. If we examine the graphical simulation for the 9% probability, the pictures show a narrow filament formed for the low repetition and forming voltage of 2.7V in 38 a). In figure 38 b) it shows the graphical representation of the highest 9% repetition at 2.9V, the filament structure is noticeably different with a wider spread at the top of the lattice structure.

Within the 5% probability of defects the lowest and highest repetition for forming voltages are shown by the graphical picture in the figures 39 a) and b) respectively. Upon close examination the figure 39 a) shows that despite broad conductive filaments form the actual conduction pathways in the structure are few and are stochastic in nature. In contrast to this the physical structure in 39 b) for the highest repetition a 5% has more complete conduction pathways in the conductive filament and the pathway are much more direct as compared to in 39 a).

In the last probability at 1% the figure 40 a) showed for one of the lowest repetition achieved at 4V. In the picture the conductive pathways geometry to be more stochastic in nature. In the preceding 5% figure 40 a) showed similar behaviour for the lower repetition of forming voltages. Figure 40 b) depicts the highest repetition at 1% of defects which has a conductive filament growing towards the top electrode unlike in 40 a) where the filament is growing towards the bottom electrode.

The following figure shows a dynamic increase in the lattice size by increasing its height. In figure 41 a) the height of the lattice is now a M =50 and N=5 and in 41 b) M = 70 and N =5. Both figures are shown for the 5% probability of defects. It is observed that by increasing hte lattice height the conductive filament is much more difficult to form even at a high forming voltage. Conversely simulating a larger lattice width than height also did not produce a conductive filament, despite being given a high probability of defects for 9%. Figure 42, shows this latter depiction for an M = 5 and N = 10 lattice structure.

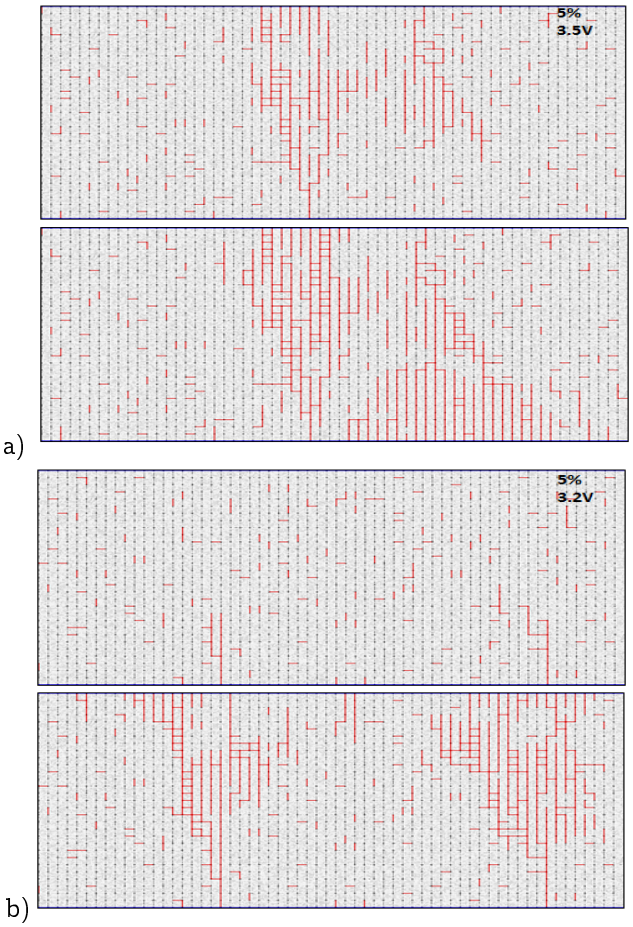


Figure 39: The pictures represent the 5% probability of defects for lowest repetition in a) and the highest in b).

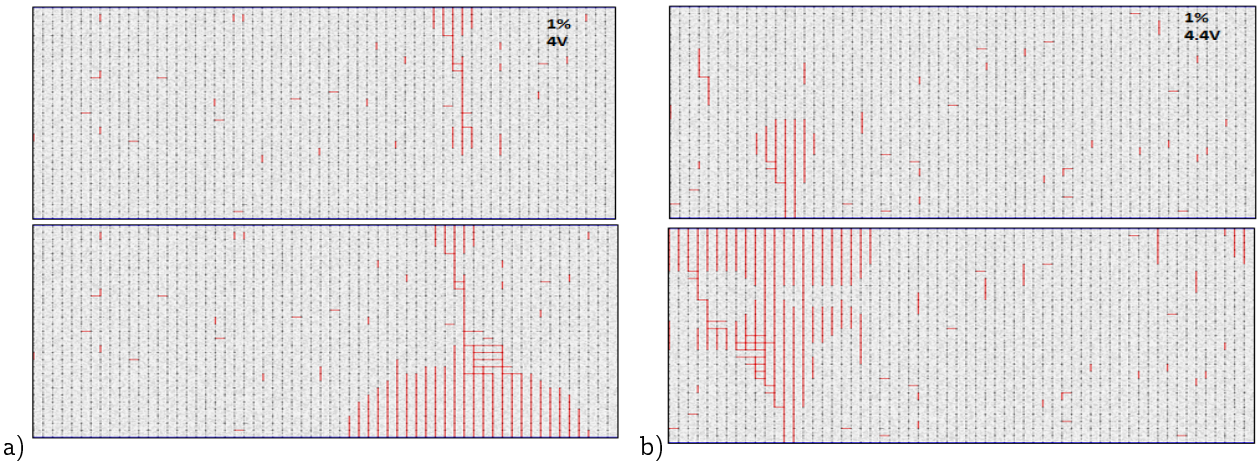


Figure 40: Both a) and b) show the 1% of defects conductive filaments formed for 2 iterations for different forming voltages.

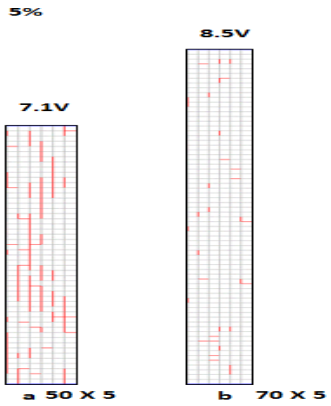


Figure 41: Increasing the height showed that higher forming voltages are needed. It is also clear that with increased height no conductive filament was formed.

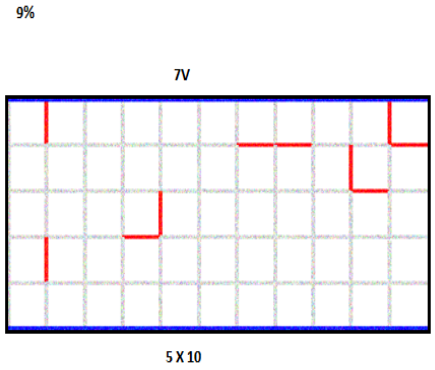


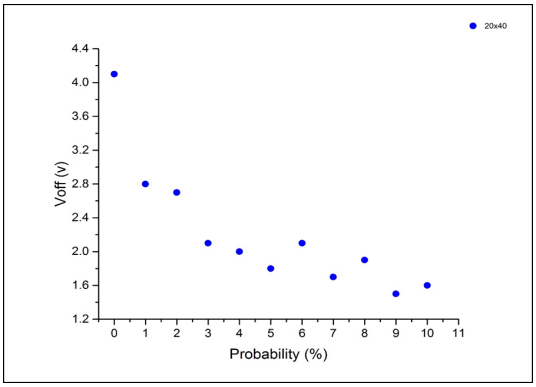
Figure 42: A lattice structure of 5 x 10 shows no conductive filament formed at 9% of defects

The successful candidates for the forming lattice structure was a close ratio between width and height.

8.2.2 RCB simulations of Voff vs Probability

Varying the lattice structure by width and height showed how the forming, RESET and SET voltages varied but the defects also plays an important role in the voltages distribution. The sample of MgO thin film can have varied pristine states where there is a different number of defects or low resistance sites throughout the oxide. Even within the same sample it was seen prior that the switching dynamics of SETs and RESETs voltages varied from device to device. The pristine state of the sample before the forming occurs can bring insights to the future behaviour of the device. The most important factor for the 3 step process is the forming. To perform the forming, the simulation is program to run like in the experiments, by obtaining the forming at a required voltage Voff.

Each device has its own unique composition of defects. We took a closer look at how the defects affected 2 device sizes. The first size comprised of a lattice structure of M = 20 and N = 40 and the second M = 20 and N = 50. The range of probability of defects increase from 0% to 10%, with 10% having the most defects

a) 

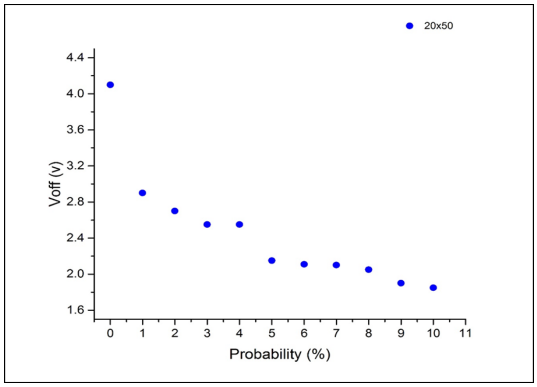
b) 

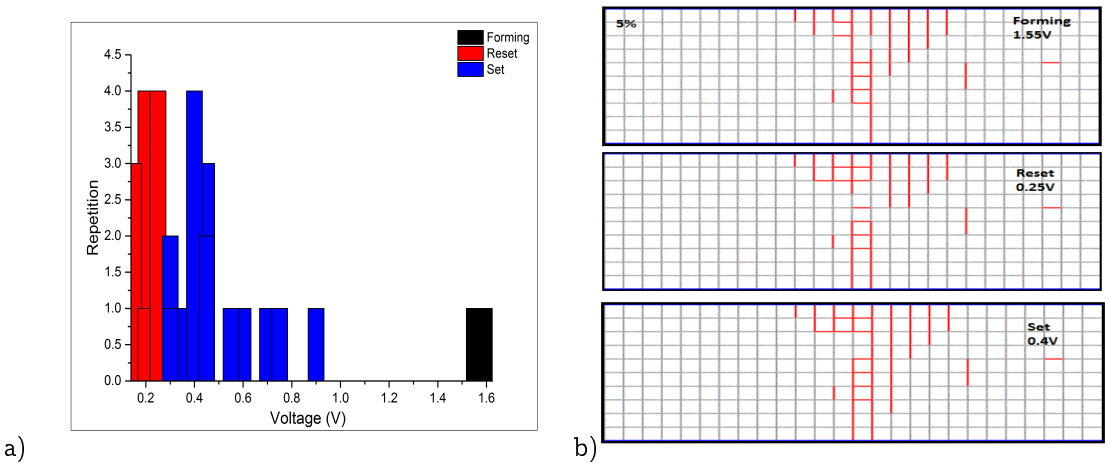
Figure 43: Different Voff voltages for 2 device sample sizes. In a) and b) there is exist the same trend of Voff decreasing exponentially with increases probability.

in both structures. In figure 43a) it is observed that as the probability increases the Voff needed for forming decreases exponentially. In figure 43 b) the same trend is apparent, but with the larger lattice structure of 20 X 50 the Voff voltages are slightly higher. The figure 43 b) lattice structure displays a smoother curve for decreasing exponentially. The ability to create localized conductive filaments by the addition of defects, increases the probability of devices having lower forming voltages Voff [13].

8.2.3 The Forming, SET and RESET process

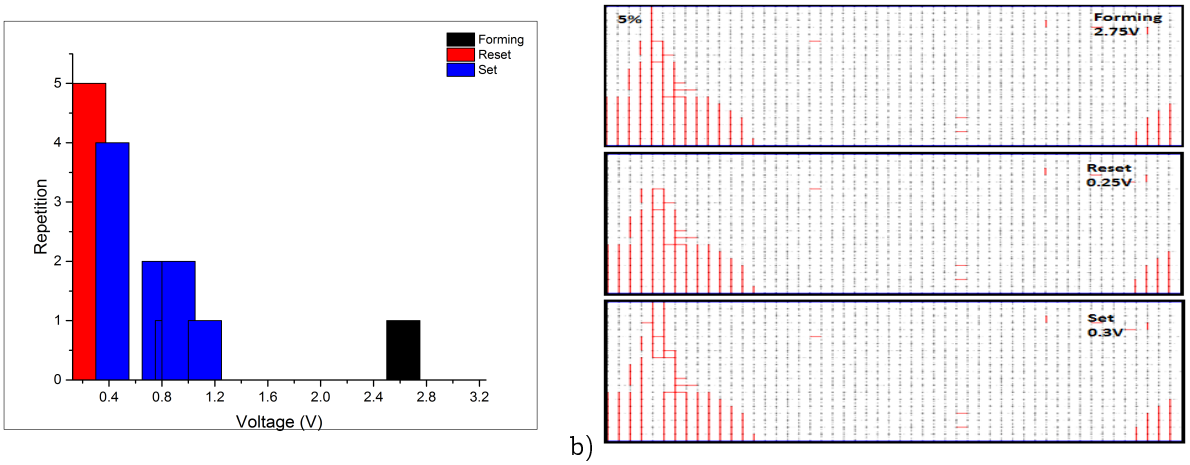
Once the forming has been performed and there is a successful conductive filament created between the top and bottom of the lattice the succeeding SET and RESET occur. This RCB simulation was done using the python code in appendix for the algorithm b). This is a 3 step process. The RESET process occurs directly after the forming since it is responsible for breaking or rupturing the conductive filament at a specific point. This process has been seen experimentally to occur at low voltages at high currents. When the RESET process has broken the conductive link a SET process occurs similar to the forming but via a lower voltage. Simulations observing a two kinds of lattice structures were performed. The first is that of a M =10 and N = 25 lattice and the second involves a thicker lattice at M = 20 and N =50 lattice structure.
In both lattice structures the overall resistance changes in the structure during the forming, SET and RESET processes. The change is that from a HRS to LRS for the forming to the RESET and a LRS to a HRS from the RESET to the SET. It is noticeable that the conductive filament is always formed in a vertical direction. The nature of the growth pattern is stochastic and the filament structures are 'tree like' in nature. The branches have been shown to exhibit an overall vertical progression of the conduction thought there exist horizontal conductive paths, but the current here is too small to contribute the overall conductive filament formed [53]. The first to be examined for this 3 step process is the smaller lattice structure of M =10 and N = 25 shown in figure 44.

The RESET has a higher repetition for 0.25V shown in figure 44 a) the forming was not high at 1.6V only. The SET process showed it can have many possibilities for creating a conductive filament. At 0.4V has the highest probability. On the right figure 44 b) shows how the 3 step process occurred. It is observed that the area of the rupturing in the conductive filament and its formation again do not occur in the same spot. In



a) b)

Figure 44: RCB simulated representation in a) of the statistical distribution of voltages for forming RESET and SET. The simulation was able to show that the SETs are the most distributed 0.3V to 0.9V as compared to the RESET and forming. In b) shows the picture representation of all 3 steps for the highest repetition voltage values.



a) b)

Figure 45: The statistical distribution for the voltages in a) for the 3 step process of forming, RESET and SET. In b) shows a picture representation of the process.

fact an entirely new conductive filament with a different structure is formed for the SET process.
Initially the forming of the complete conductive filament reaches a LRS state. The RESET occurs at the part of the filament referred to as the 'hottest bond' [45], which is a broken area in the conductive filament where no current can flow. This results in a HRS state. The SET process begins in the area of the HRS.
The second simulation for this 3 step process shown in figure 45, is the lattice size with M = 20 and N = 50. The lattice structure is embedded with 5% probability of defects. The forming occurs for one distribution value of 2.75V. The RESET begins at this LRS to rupture the bond. The RESET occurs at 0.25V as before for the smaller lattice structure. The SET process begins to reform the broken conductive filament at the HRS state. This is more likely to occur at 0.3V for the SET process, which is noticeably smaller than the forming voltage. in figure 45 b) the picture shows how the process occurs, again the SET conductive filament differs from the original forming process filament.

8.2.4 Conclusion

We designed a computer program using python to produce an RCB network mode. Our computer model successfully produced simulations mimicking the forming, RESET and SET processes in the oxide. The program considered an MxN lattice made up of bonds of a low resistive state to a high resistive state. Each bond changed its state of $\triangle v$ by the application of an external voltage value. The process of forming, process was formed at a single Voff value, whereas the RESET or SET was formed by a slight increase in voltages till the Voff value. The program produced a statistical distribution of repetition versus voltages for each of the processes and in relation to that pictures of the actual growth of the conductive filament. The conductive filament were irregular in shape, having a 'tree like' nature, with many stochastic branches. It was noticed that the conductive filament had both vertical and horizontal conductive pathways but only the vertical pathway influenced the growth pattern from top tp bottom or bottom to top in the lattice. Based on the filament shape it may be too irregular where no straight line of bonds produce assimilate to have a conductive pathway. It has been postulated that more than one conductive filament is formed and this is seen here in our simulations, still it is unclear if multiple filaments formed contribute to the conductivity of the device. The nature of the conductive filament is realized to change for multiple iterations, indicating that each device in a sample has its own signature conductive filament, each different in geometry. The RCB model is successful in producing the reversible process in resistive switching.

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Part V
Conclusions and Future Work

The resistive switching random access memory (ReRAM) device using MgO showed successful switching behavior. MgO was used as the insulator for the metal-insulator-metal (MIM) structure because of its high dielectric constant. MgO ReRAM devices showed effective reproducible switching and were classed as generic memristors that exhibited unipolar switching. As unipolar switching devices there existed some variability found in the switching distribution cycles for SETs and RESETs.

One role was to understand why this recurrence of variation between the SET and RESET voltages occurred. The success of ReRAM devices is controlling this major factor. As ReRAM devices made from binary metal oxides, the key is to control the mobility of the oxygen ions in the device that serve as the conductive filament. There are many proposals such as inserting a second metal layer at the interface, inserting defects, and adjusting scalability. The latter proposal was studied through the varied thickness of the MgO films in four samples. The ReRAM devices were fabricated using a sputtering technique by INESC.MN (Lisbon) PVD-Magnetron, for a total of four samples. Each sample was designed using the metal-insulator-metal structure typical for ReRAM devices. The samples were labelled from S1, S2, S3 and S4 and ranged from 15nm, 30nm, 22.5nm and 40nm respectively. Each sample consisted of individual memristive devices, with a total of thirty six (36) in number. Attaining the individual devices was decided upon the use of a shadow mask. The shadow mask was inserted near the top active electrode of tantalum to create a patterned thin film. The use of the shadow mask provided superior control of lateral spacing in the sizing of the individual devices. Each device had the possibility to be scaled to 300µm and showed as topographical changes in the form of circular discs. The rationality of having individual devices laid in the assumption that, the sample may not be homogenous throughout, in providing a higher degree of micro-scaling, and the ability for easier electrical testing.

The electrical testing allowed for the characterisation of the samples by non-volatility, scaling, endurance, operating voltage, switching scheme of either unipolar or bipolar and conduction mechanisms. All of which, gave insights into the cell performance of the ReRAM devices, for easier identification of the optimum design sample.

The numerous I/V tests performed on these samples were done using a two microprobes and a Keithley source meter. Real-time observation of electrical behavior was provided by a LABVIEW program. The real-time observation revealed hysteresis loops formed, which Leon Chua proposed to identify memristive behavior of history dependence on resistance. As the I/V tests were undertaken, caution was adhered to for the prevention of a full dielectric breakdown of our MgO film. Since MgO has a high dielectric constant it allowed for a wider range of applied voltages before instigating a full breakdown of the device. It was one of the reasons MgO was chosen. It became apparent under testing; the choice of MgO showed two forms of switching schemes, unipolar and

bipolar with a predominance of unipolar switching observed in three samples having the greater thicknesses.

By the application of voltage steps, the electroforming was performed. An applied high electrical stress imposed, showed that through the electroforming step a physical change occurred in the form of a SET. It has been previously reported and shown within our experiments; that within the dielectric MgO, the temporary conduction state is due to the migration of oxygen ions. The conduction mechanisms identified were hopping conduction and space charge limited conduction moving along a percolated path. This electroforming step for our device showed it was a prerequisite for RESETs and SETs cycle succession in thicker oxides and negligible for the succession in the thinner oxides.

Endurance testing conducted showed the reproducibility of cycles for the samples, each having a minimum average of fifty cycles for each applied voltage schemed bias. Studies were also undertaken to see the full endurance for devices in samples before fully demolishing. This showed to be approximately 370 cycles of SETs and RESETs succession under positive voltage scheme.

The breakdown of the samples can be related to the increased number of electron traps. As MgO is a gate oxide the increase in the charge trap density is directly related to the thickness of the oxide. MgO film of greater thickness had longer endurance cycles corresponding to less charge trap areas. Since progressively occurring voltage sweeps do not significantly alter the device the initial first voltage sweep plays a major role in the generation of defects. Thus it was realized that a higher voltage sweep in the beginning of the forming step can affect the endurance of the device, still this is not limited to the only cause responsible for the breakdown of the devices in samples.

The procedure for endurance testing highlighted the nature for SETs and RESETs. As such, the variability of the SET-RESET switching was also addressed. The use of a simple percolation model attested to providing an understanding of the switching distribution within our devices. The random circuit breaker network model (RCB) was created using a python program. There were two versions, one that looked solely on producing simulations of the electroforming process and the other which encompassed this step but followed for the RESET and SET process. It was realized through the computer simulations of the RCB model that the electroforming process added further defects within the oxide which can add to enhance variability in switching dynamics.

The electroforming process created conductive filaments that were previously thought in some studies to be one conductive path. These conductive filaments varied in number from 1 to 3 filaments in some samples. The simulated conductive filament geometry had a 'tree-like' or 'dendrite' appearance in all simulated samples. The stochastic patterns of the conductive filament showed the ability to provide increased complexity to resistive switching behavior. If the electroforming step can be eliminated there can improved resistive switching dynamics. This study provided insights into the stochastic nature of resistive switching for one of the most promising materials used in ReRAM devices.
Large Roff/Ron ratio, and reduce variability of SETs and RESETs switching distribution. The scalability of the MgO ReRAM devices played a crucial role for enhanced ReRAM device operation. It was realized that SET voltage was heavily reliant upon the thickness of the MgO.

To continue work in this area would aid the scientific community in building a further understanding of ReRAM devices that can eventually lead to the successful replacement of flash memory devices. ReRAM devices show the potential to become the future of nonvolatile memory.

Future work

- ⊗ To continue RCB model simulations for more complex design fabrication of MIM structures.
- ⊗ To fabricate devices with a range of thickness scalability near the most successful sample candidate
- ⊗ To eliminate the electroforming process in oxides used in MIM structures.
- ⊗ To study the 'tree-like' or 'dendrite' nature of the conductive filament for any emergent patterns, that can be predicted in these shapes.

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Algorithm 1 Python code for simulating the behaviour of the forming and conductive filament in ReRAM devices for revsisble dynamics.

An adaptation of Chae's RCB code was written by Catarina Dias. The codes were designed using the python program.

```
# -*- coding: utf-8 -*-
"""
Created on Mon Apr 13 14:52:43 2015
@author: Catarina Dias
"""
from ahkab import new_ac, new_op, run, devices
from ahkab.circuit import Circui
from ahkab.plotting import plot_results # calls matplotlib for you
import numpy as np
from random import*
from PIL import Image, ImageDraw
import matplotlib.pylab as plt
from collections import Counter
from collections import OrderedDict
import os
#V=R*I
Roff=1000
Ron=1
p=0.005 #% (probability of initial defects)
Icomp=50 #A (fixed in the paper)
Icomp2=5. #A (for the RESET and SET process)
#von>>voff
voff=3
von=0.2 #1 -> 7V; 3 -> 8V
#it was assumed the absolute value of the voltage differential for boundary conditions,
#since it can "switch" in either direction
#Source voltage parameters
Vmax=10.
Vmin=0.
deltaV=0.1
#set ratio (for iteration to stop)
ratioS=10.
#MxN network
M=10 #rows
N=25+1 #coulmns (it counts less one column by default)
#for more than 20x20 to work, the value dense_matrix_limit in file options.py (line 65) was changed
#from 400 to 2000 because otherwise there was an error when creating the sparse matrix
#n file dc_analysis.py (line 797)
#for drawing
s=50 #scaled up by 10
#if M=3 and N=2:
# ——————————
# R1 R3
# R2
# R4 R6
# R5
# R7 R8
# ——————————
#draw the circuit
def draw_circ(S,Rs,s,step,it,v):
```

Algorithm 2 Python code for simulating the forming, RESET and SET process for reversible dynamics.

An adaptation of Chae's RCB code was written by Catarina Dias. The codes were designed using the python program.

```
# -*- coding: utf-8 -*-
"""
Created on Mon Apr 13 14:52:43 2015
@author: Catarina Dias
"""
from ahkab import new_ac, new_op, run, devices
from ahkab.circuit import Circuit
from ahkab.plotting import plot_results # calls matplotlib for you
import numpy as np
from random import*
from PIL import Image, ImageDraw
import matplotlib.pylab as plt
from collections import Counter
from collections import OrderedDict
#V=R*I
Roff=1000
Ron=1
p=0.05 #% (probability of initial defects)
Icomp=50 #A (fixed in the paper)
Icomp2=5. #A (for the RESET and SET process)
#von>>voff
voff=3.5
von=1.5
#it was assumed the absolute value of the voltage differential for boundary conditions,
#since it can "switch" in either direction
#Source voltage parameters
Vmax=100.
Vmin=0.
deltaV=0.5
#switching ratio (for iteration to stop)
ratioF=20.
ratioR=10.
ratioS=10.
#MxN network
M=20 #rows
N=30+1 #coulmns (it counts less one column by default)
#for more than 20x20 to work, the value dense_matrix_limit in file options.py (line 65) was changed
#from 400 to 2000 because otherwise there was an error when creating the sparse matrix
#n file dc_analysis.py (line 797)
#for drawing
s=50 #scaled up by 10
#if M=3 and N=2:
# ————————————
# R1 R3
# R2
# R4 R6
# R5
# R7 R8
# ————————————
#draw the circuit ————————————————————————————————————————————————————————————
def draw_circ(S,Rs,s,step,it,v,boundary):
```

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